

AMS-02 GDAQ  
JHIF Flight-Version Board  
Hardware Design Specification

# Approval and Signature

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JHIF Flight-Version Board Hardware Design Specification

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## Document Revision Record

No.	History	Date	Remark
01	Initial Issue	April 20, 2002	
02	• 5 : Updated <i>CONNECTOR PIN ASSIGNMENT</i> description	June 12, 2002	
03	• 2.2 : Updated <i>JFOM Module</i> description • FIGURES : Updated Figure-1、Figure-3 and Figure-6	July 24, 2002	
04	• 2 : Updated <i>FEATURE</i> description • FIGURE : Updated Figure-1 • APPENDIX : Added <i>Appendix</i> description and Data File	Oct. 15, 2002	

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## 1. SCOPE

This document provides information about the feature and operation specification of the JHIF (High-Rate Interface) flight-version board in AMS-02 GDAQ system. AMS is designed to measure the amount of antimatter nuclei present in cosmic rays. The GDAQ system is used to process data collected from front sensors.

The GDAQ system contains three data acquisition and processing levels: the front-end DAQ, the intermediate DAQ and the top-level DAQ. The processing element of the top-level DAQ is MDC. JMDC receives concentrated data from intermediate DAQ via AMS-Link, performs data processing and then passes framed data to ISS via fiber optic links. The MDC is composed of three 6U compact PCI boards, a JSBC board to process data, a JBU board to store data and a JIM board to communicate with other modules. The redundancy consideration of top-level DAQ system is implemented via four JMDCs.

The JHIF board has two types of modules, a J422 type module and a JFOM type module. The J422 module communicates among four JIM-422 boards and two RS-422 interfaces. The JFOM module communicates among four JIM-HRDL boards and two FO (Fiber Optic) interfaces. There are two independent JFOM modules in the JHIF board. Only one JFOM module will be powered and operated at one time.

## 2. FEATURE

### 2.1 J422 Module

- Differential Line Receiver (AM26LS32)
- Differential Line Driver (AM26LS31)
- Wired-OR Buffer

Open Collector Buffer (5407)

Passive Components

### 2.2 JFOM Module

- Data Link Receiver (Teledyne 2302215-1)

Nominal Operating Wavelength 1300 nm

Maximum Data rate 125 MBd

Data output is differential ECL

Signal-Detect output is single-ended ECL or PECL

- Data Link Transmitter (Teledyne 2302220-1)

Nominal Operating Wavelength 1300 nm

Maximum Data rate 125 MBd

Differential ECL or PECL data input

Single-ended ECL or TTL device-enable input

- RX Fan-Out Mechanism

ECL 1:2 Differential Fan-Out Buffer (MC10EP11)

ECL to TTL Translator (MC10ELT25)

NPN Transistor (2N2222A)

Passive Components

- Receiver and TX Logic-OR Mechanism

ECL 2-Input Differential AND/NAND (MC10EP05)

Differential ECL Receiver/Driver (MC10EP16)

TTL to ECL Translator (MC10ELT24)

NPN Transistor (2N2222A)

Passive Components

- Dallas Temperature Sensor

4 Dallas Sensors

- Front Panel

### 3. ARCHITECTURE

#### 3.1 Block Diagram

The detailed block diagrams of JHIF board are shown in Figures 1-7.

#### 3.2 Functional Description

The JHIF board transmits and receives data among four JIM-422s and two RS-422 interfaces and among four JIM-HRDLs and two FO interfaces. Major functions of the JHIF board are Wired-OR, Fan-Out, Logic-OR, data buffering and data transceiving.

##### 3.2.1 J422 Module

###### 3.2.1.1 RX Path

Four differential TTL signals, from two RS-422 interfaces, are received by the Differential Line Receiver to generate four single-ended TTL signals. Each RS-422 interface contains two types of differential TTL signals (data and clock). These four single-ended TTL signals are sent to the Wired-OR Buffer (Figure-2) through the open collector buffer and are hard-wired together to generate two single-ended TTL signals. These two single-ended TTL signals are directly fanned-out to generate eight single-ended TTL signals (two sets of one-to-four fan-out) and are sent to the Differential Line Driver. Outputs of the Differential Line Driver (eight differential TTL signals) are used to directly drive four JIM-422 boards.

###### 3.2.1.2 TX Path

Eight differential TTL signals from four JIM-422 boards are sent to the Differential Line Receiver to generate eight single-ended TTL signals.

These eight single-ended TTL signals are sent to the Wired-OR buffer through the open collector buffer and are hard-wired together to generate two single-ended TTL signals. These two single-ended TTL signals are fanned-out to generate four single-ended TTL signals (two sets of one-to-two fan-out) and are used to directly drive Differential Line Driver. Differential Line Driver generates four differential TTL signals and sends them to two RS-422 interfaces.

### 3.2.2 JFOM Module

There are two JFOM modules in the JHIF board, and they can operate independently. Each JFOM module contains RX path circuitry and TX path circuitry.

#### 3.2.2.1 RX Path

The optical signal from FO interface is received by the Data Link Receivers to generate a differential ECL RX (Receive Data) signal and a single-ended ECL SD (Signal-Detect) signal. These two signals are sent to the RX Fan-Out Mechanism (Figure-3). In the RX Fan-Out Mechanism, the RX signal is sent to the two-layer of Fan-Out Buffer to generate four differential ECL signals. These four differential ECL signals are sent to the corresponding JIM-HRDL board. The SD signal is sent to the ECL-to-TTL Translator to generate a TTL signal. This TTL signal is sent to the SD Fan-Out Buffer (Figure-4) to generate four TTL signals. These four TTL signals are sent to the corresponding JIM-HRDL board.

In the RX path, the SD signal is generated by the JHIF-JFOM module and is used to control the transmission of the RX signal. This control

function (ECL Logic-AND of SD signal and RX signal) is implemented on the JIM-HRDL board.

### 3.2.2.2 TX Path

Four groups of signals from four JIM-HRDL boards, pass through the M-signal Interface (Figure-5) and the ECL Differential Receiver, are sent to the TX Logic-OR Mechanism (Figure-6). Each group contains a single-ended TTL M (control) signal and a differential ECL TX (data) signal. The M-signal is sent to the TTL-to-ECL Translator to generate a differential ECL signal. These four groups of two differential ECL signals are sent to four ECL AND gates. Four ANDed differential ECL signals are sent to the two-layer of Logic-OR gate to generate a differential ECL signal. This differential ECL signal is used to drive a Data Link Transmitter to generate an optical signal for the FO interface.

In the TX path, the M-signal is generated by the JIM-HRDL board and is used to control the transmission of its TX signal. Only one M-signal will be active (TTL logic high) at one time.

### 3.2.2.3 Terminator

For the purpose of implementing ECL signals termination and output biasing, a terminator is inserted into the input of the ECL devices (denoted by the “T” symbol as shown in Figure-3 and Figure-6). The Y-termination method is used to implement this function. Figure-7 shows the circuitry of the terminator.

## 4. TEST

A test board for simulating the interface function of JIM-422 and JIM-HRDL is used to perform the function test of the JHIF board. We self-loop the RS422 interface to verify the J422 closed-loop function and self-loop the FO interface to verify the JFOM closed-loop function. The block diagram of the JHIF board test is shown in Figure-8.

### 4.1 J422 Module Test Procedures

- (1) Connect the interface signals between J422 and J422\_Test (TXC, TXD, RXC and RXD Signals).
- (2) Self-Loop the RS422 interface of J422 (Connect 422\_TX to 422\_RX).
- (3) Insert the test pattern into the TX\_Test terminal on the J422\_Test.
- (4) Receive the signal from the RX\_Test terminal on the J422\_Test.
- (5) Verify the insert pattern and the received pattern.

### 4.2 JFOM Modules Test Procedures

- (1) Connect the interface signals between JFOM and JFOM\_Test (M, TX and RX signals).
- (2) Self-Loop the FO interface of JFOM (Connect FO\_TX to FO\_RX).
- (3) Insert the test pattern into M\_Test and TX\_Test terminals on the JFOM\_Test.
- (4) Receive the signal from RX\_Test terminal on the JFOM\_Test.
- (5) Verify the insert pattern and the received pattern.

## 5. CONNECTOR PIN ASSIGNMENTS

Connectors P1, P2, P3, and P5 are not used in the JHIF board. The pin assignments of connector P4 are listed as follows.

	Pin	Z	A	B	C	D	E	F
P4	25	GND	+5V_B	RXLB1+	RXLB2+	RXLB3+	RXLB4+	GND
	24	GND	+5V_B	RXLB1-	RXLB2-	RXLB3-	RXLB4-	GND
	23	GND	AGND	RXLA1+	RXLA2+	RXLA3+	RXLA4+	GND
	22	GND	-5.2V_B	RXLA1-	RXLA2-	RXLA3-	RXLA4-	GND
	21	GND	-5.2V_B	TXLB1-	TXLB2-	TXLB3-	TXLB4-	GND
	20	GND	AGND	TXLB1+	TXLB2+	TXLB3+	TXLB4+	GND
	19	GND	+5V_A	TXLA1-	TXLA2-	TXLA3-	TXLA4-	GND
	18	GND	+5V_A	TXLA1+	TXLA2+	TXLA3+	TXLA4+	GND
	17	GND	AGND	AGND	AGND	AGND	AGND	GND
	16	GND	-5.2V_A	MUX12	MUX22	MUX32	MUX42	GND
	15	GND	-5.2V_A	MUX11	MUX21	MUX31	MUX41	GND
N	12-14	KEY AREA						
E C T O R	11	GND	GND	SD12	SD22	SD32	SD42	GND
	10	GND	+5V_4	SD11	SD21	SD31	SD41	GND
	9	GND	+5V_4	GND	GND	GND	GND	GND
	8	GND	CHGND	TXC1-	TXC2-	TXC3-	TXC4-	GND
	7	GND	CHGND	TXC1+	TXC2+	TXC3+	TXC4+	GND
	6	GND	TEMP1_VDD	TXD1+	TXD2+	TXD3+	TXD4+	GND
	5	GND	TEMP1_DQ	TXD1-	TXD2-	TXD3-	TXD4-	GND
	4	GND	TEMP1_GND	RXD1+	RXD2+	RXD3+	RXD4+	GND
	3	GND	TEMP0_VDD	RXD1-	RXD2-	RXD3-	RXD4-	GND
	2	GND	TEMP0_DQ	RXC1-	RXC2-	RXC3-	RXC4-	GND
	1	GND	TEMP0_GND	RXC1+	RXC2+	RXC3+	RXC4+	GND
	Pin	Z	A	B	C	D	E	F

AGND and GND will be bridged in moat.

## 6. POWER REQUIREMENTS

The JHIF board needs five independent power supplies. The estimated power supply currents are listed as follows.

### 6.1 J422 Module (See Table-1)

+5V\_4: 400 mA (nor), 631 mA (max)

### 6.2 JFOM Modules (See Table-2)

+5V\_A: 112 mA (min), 131 mA (nor), 170 mA (max)

+5V\_B: 112 mA (min), 131 mA (nor), 170 mA (max)

-5.2V\_A: 1142 mA (min), 1306 mA (nor), 1512 mA (max)

-5.2V\_B: 1142 mA (min), 1306 mA (nor), 1512 mA (max)

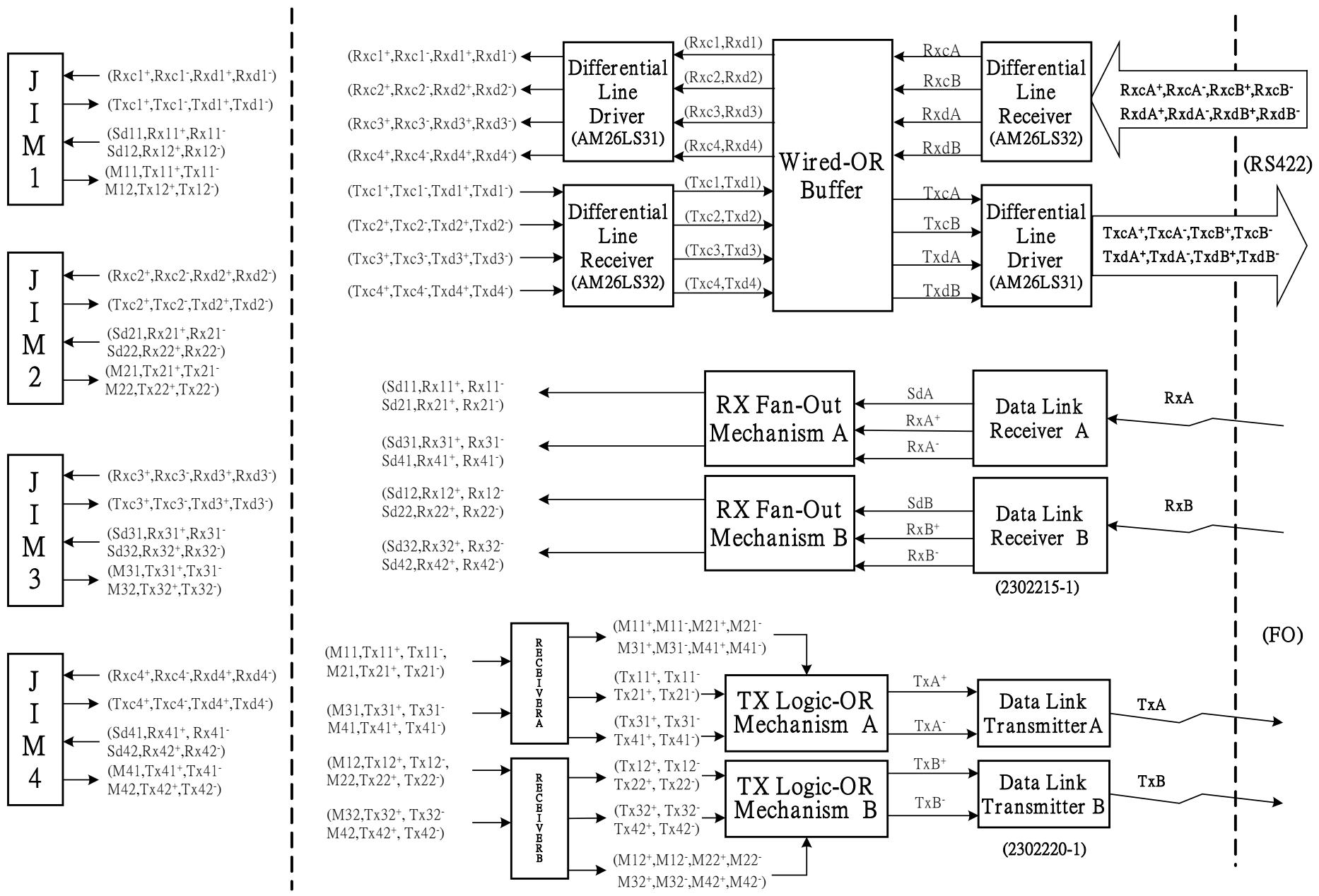
Table-1 Power Supply Currents of JHIF Board (J422)

Item	No.	P/S	Current (mA)			Current (Sub_Total)		
			min	nor	max	min	nor	max
AM26LS31M	3	+5V		32	80		96	240
AM26LS32M	3	+5V		52	70		156	210
5407	3	+5V		30	41		90	123
Passive Components		+5V					58	58
Total		+5V					400	631

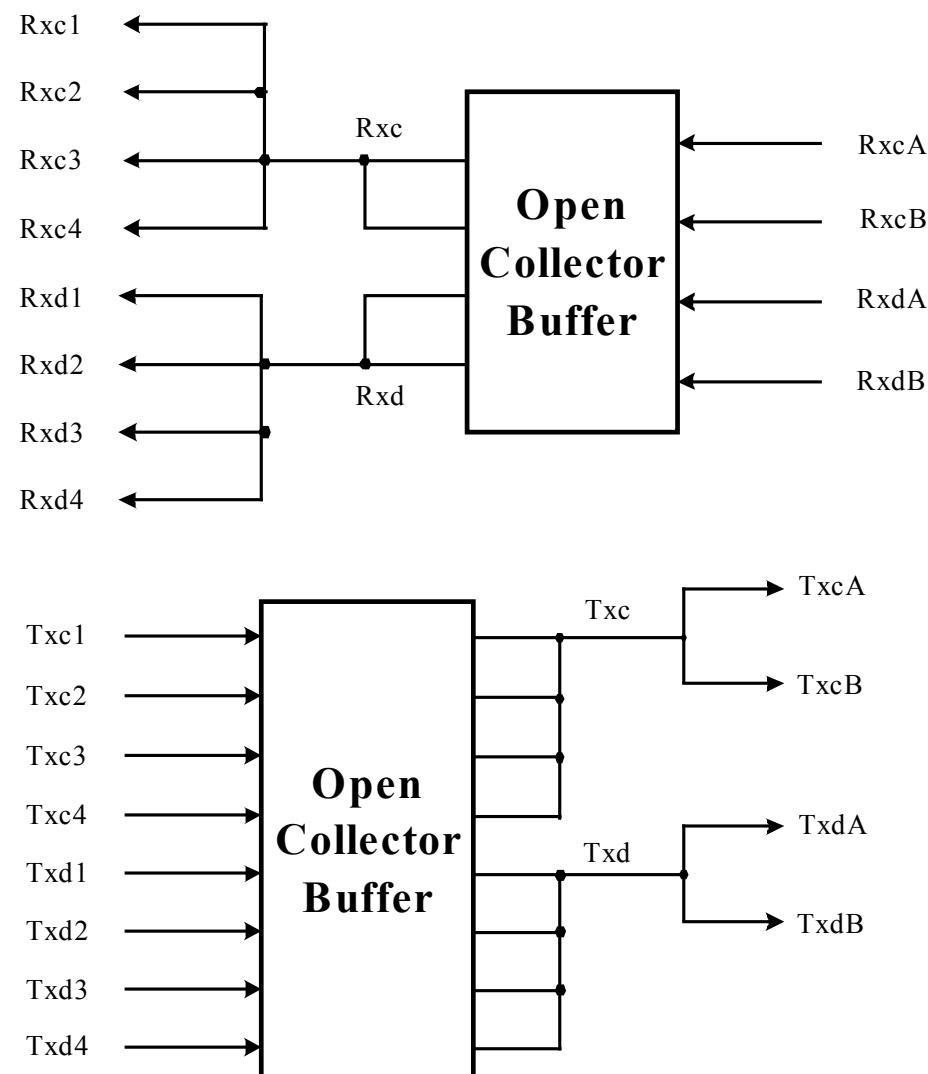
Table-2 Power Supply Currents of JHIF Board (JFOM)

Item	No.	P/S	Current (mA)			Current (Sub-Total)		
			min	nor	max	min	nor	max
2302205-1T	1	-5.2V	114	180	245	114	180	245
2302210-1R	1	+5V	75	94	112	75	94	112
		-5.2V	80	104	127	80	104	127
2N2222A	8	+5V		3	5		24	40
MC10EP05	7	-5.2V	20	24	29	140	168	203
MC10EP11	3	-5.2V	20	30	39	60	90	117
MC10EP16	4	-5.2V	20	24	31	80	96	124
MC10ELT24	4	-5.2V		12.5	18		50	72
MC10ELT25	1	+5V		13	18		13	18
		-5.2V		15	21		15	21
Passive Components		-5.2V					603	603
Total		+5V				112	131	170
		-5.2V				1142	1306	1512

Figure-1 JHIF System Block Diagram



## Figure-2 Wired-OR Buffer



# Figure-3 RX Fan-Out Mechanism

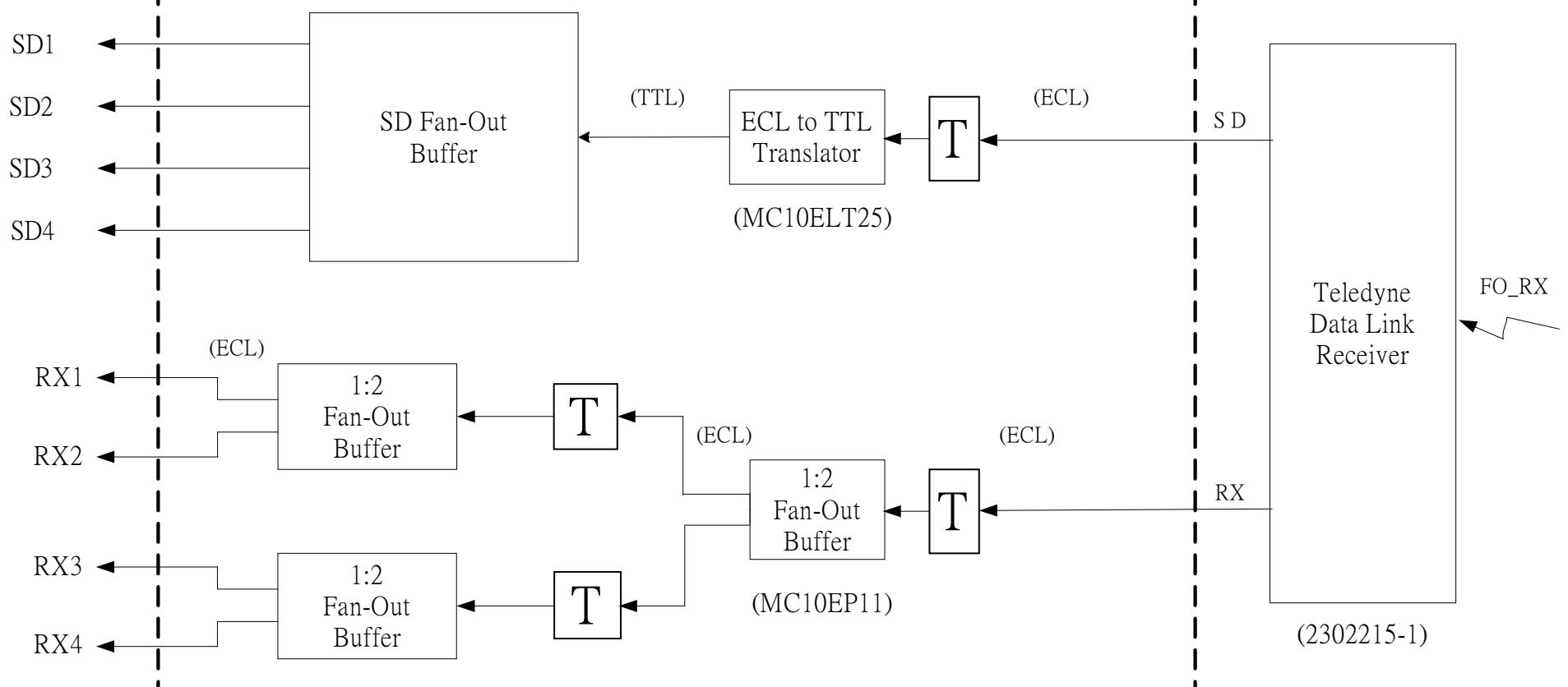


Figure-4 SD Fan-Out Buffer

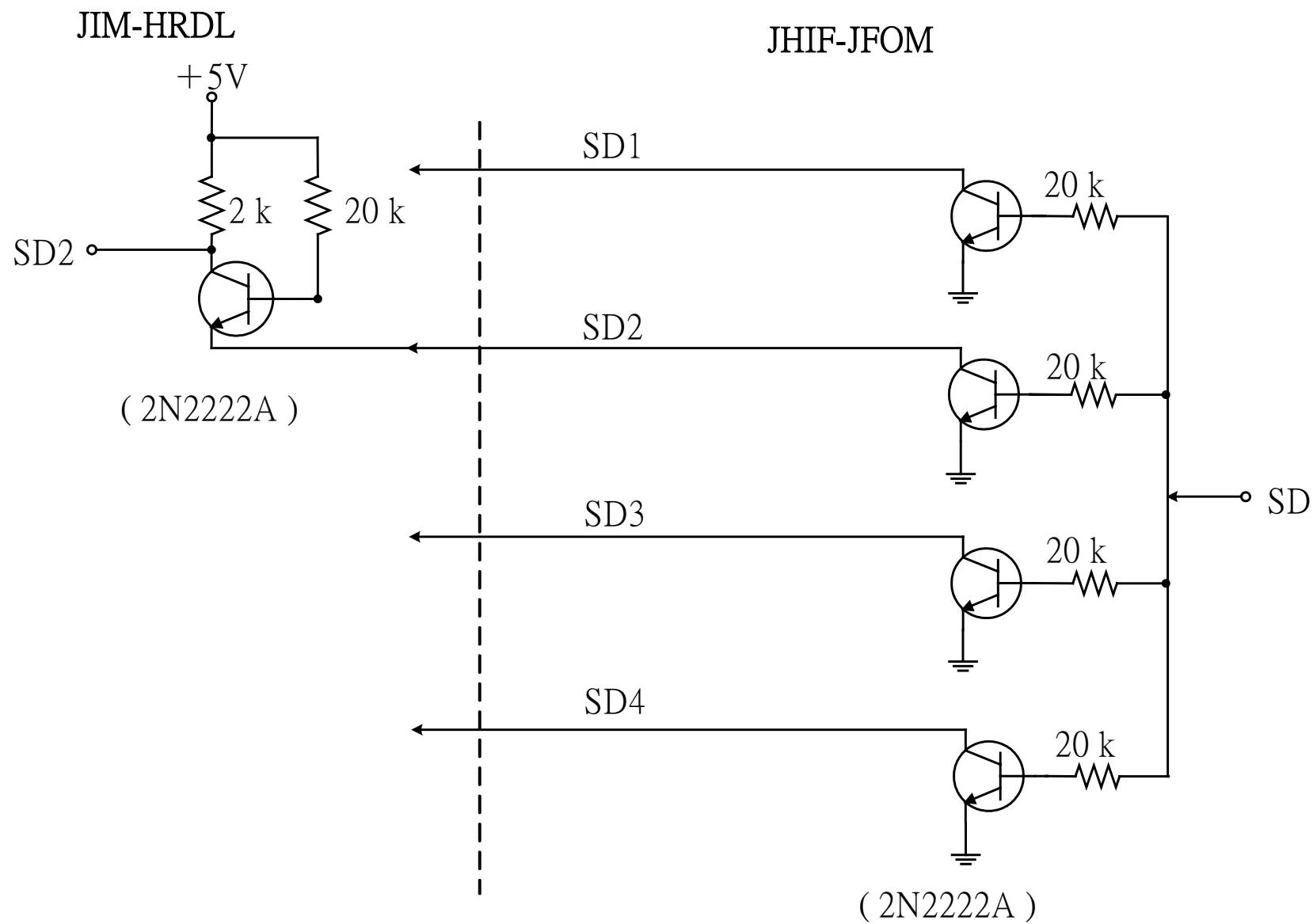
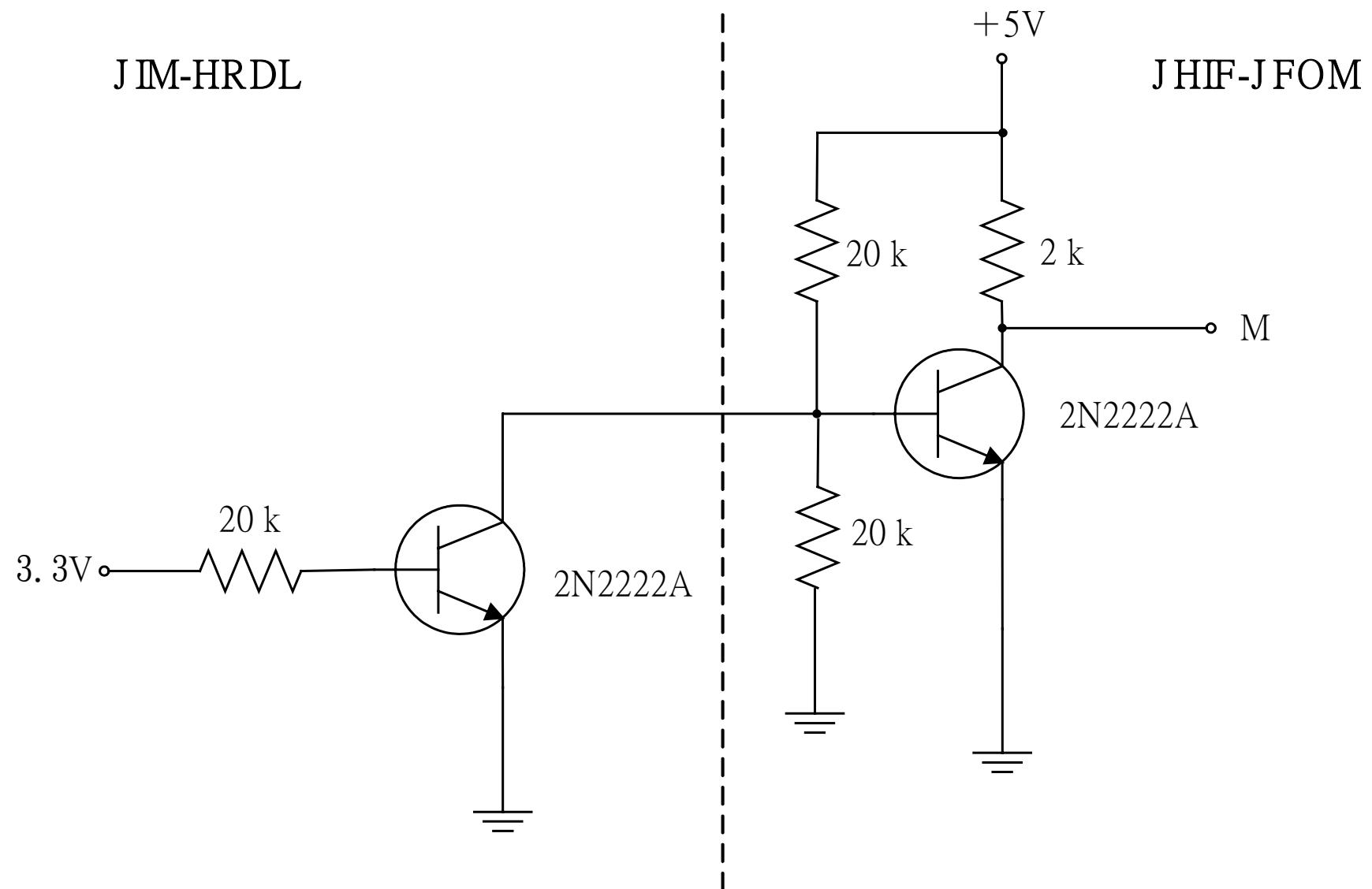
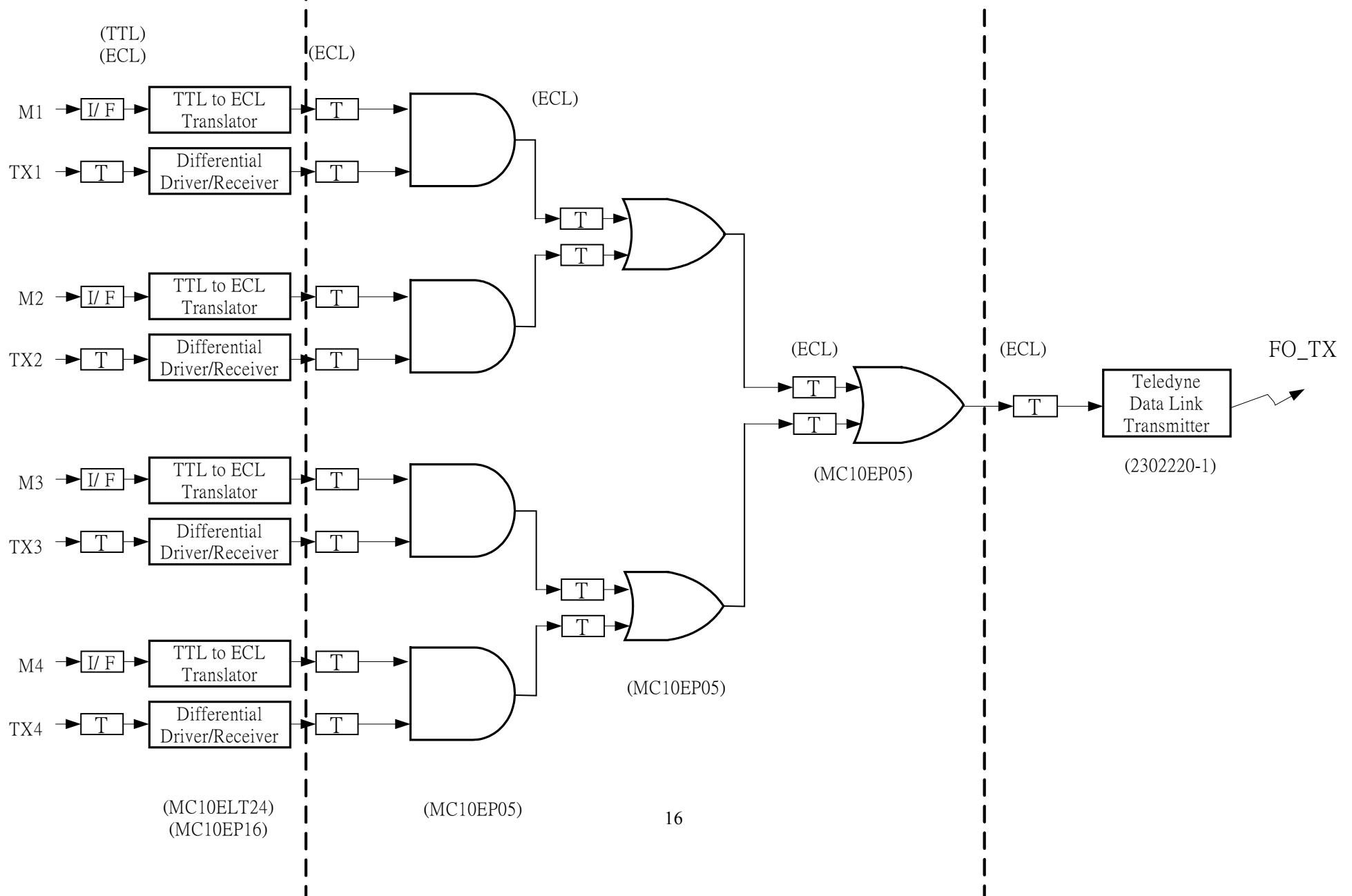


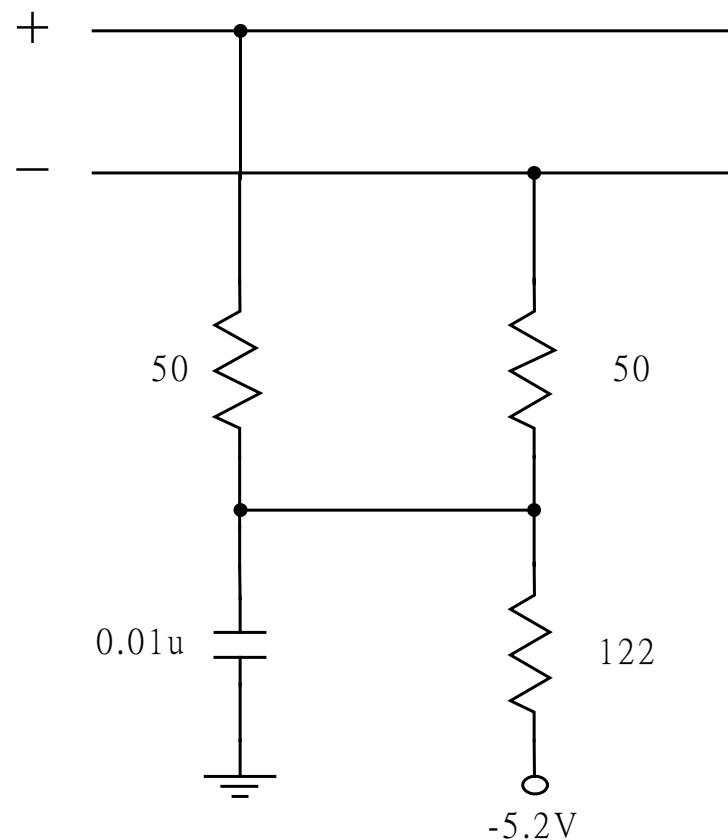
Figure-5 M-Signal Interface



# Figure-6 Receiver and TX Logic-OR Mechanism

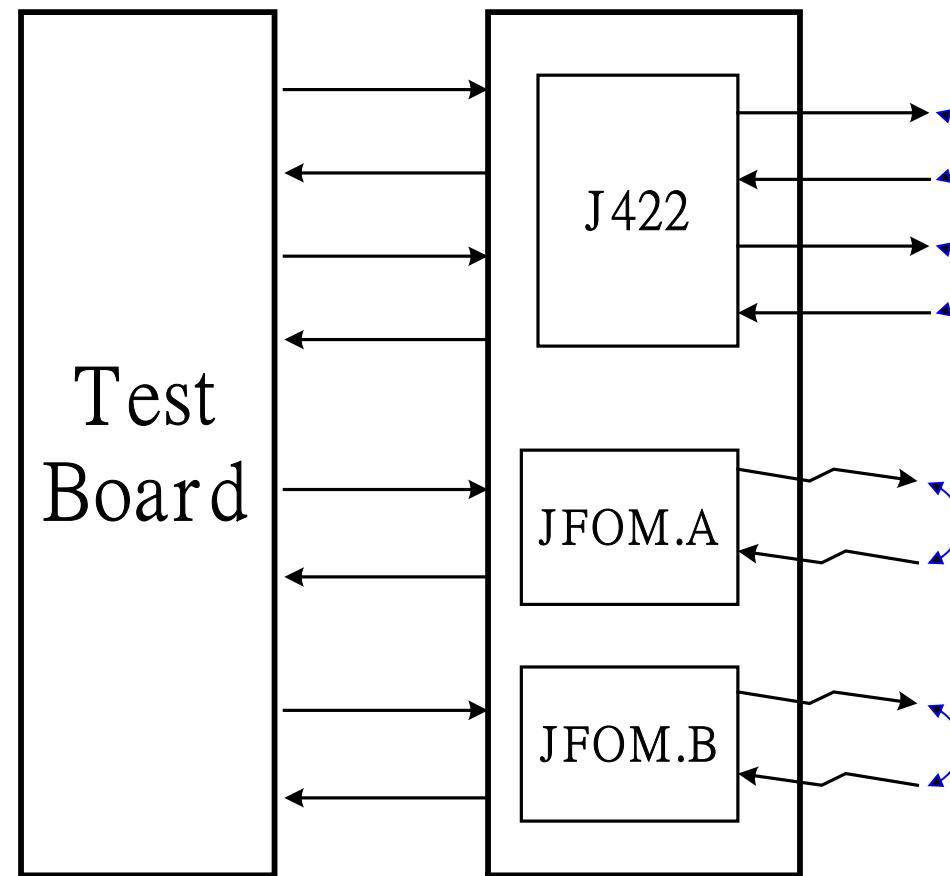


## Figure-7 Terminator



Y-Termination

Figure-8 Self-Loop Test of JHIF Board



## GLOSSARY

AMS	Alpha Magnetic Spectrometer
ECL	Emitter Coupled Logic
FO	Fiber Optic
GDAQ	Global Data Acquisition System
HRDL	High Rate Data Link
ISS	International Space Station
J422	RS-422 Multiplexer
JBU	JMDC Memory Buffer board
JFOM	Fiber Optic Multiplexer
JHIF	JMDC High-Rate Interface board
JIM	JMDC Interface Module board
JMDC	Master DAQ Computer
JSBC	JMDC Single Board Computer board
PCI	Peripheral Component Interconnect
TBM	To Be Modified
TTL	Transistor Transistor Logic

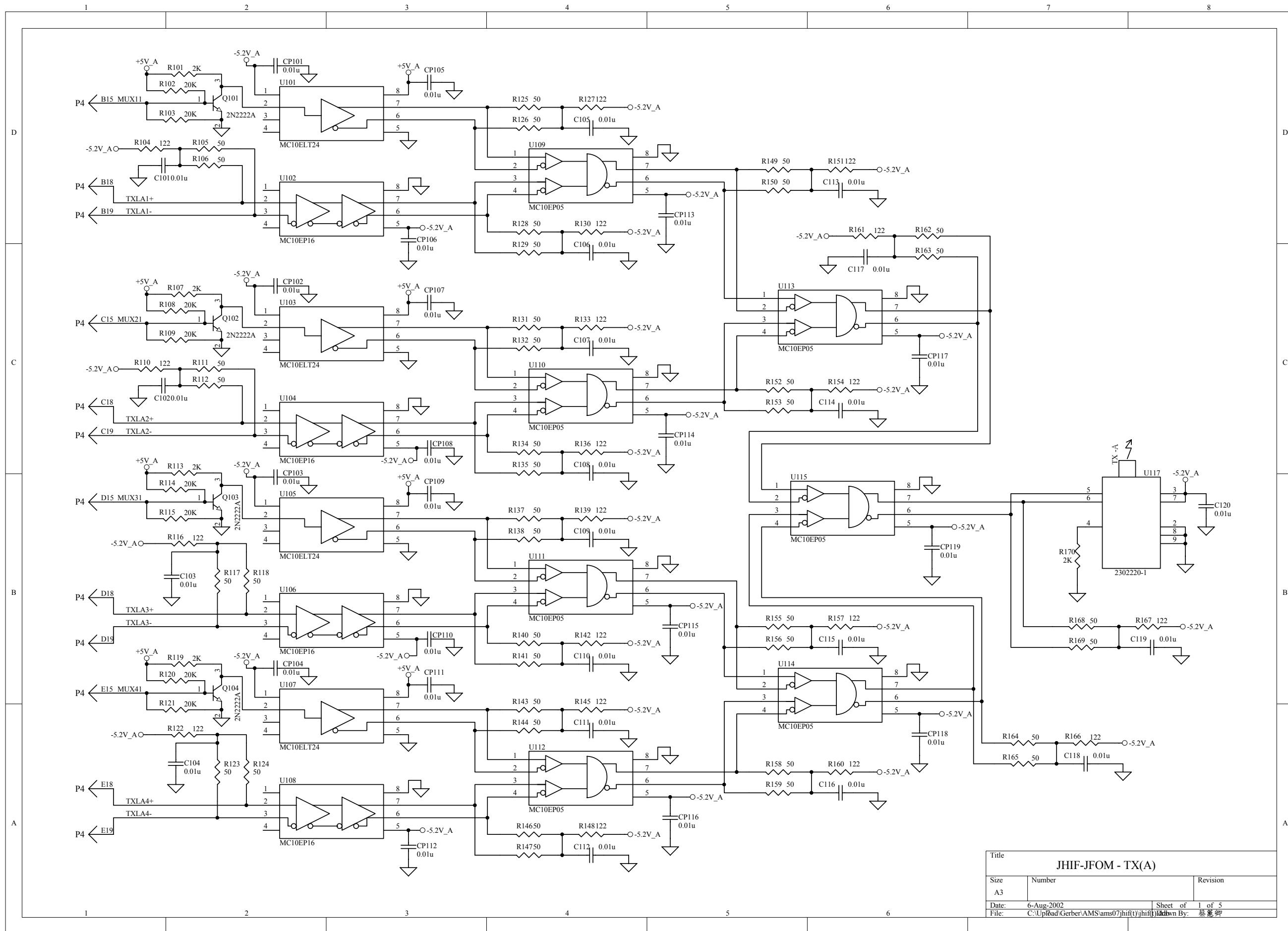
## **APPENDIX**

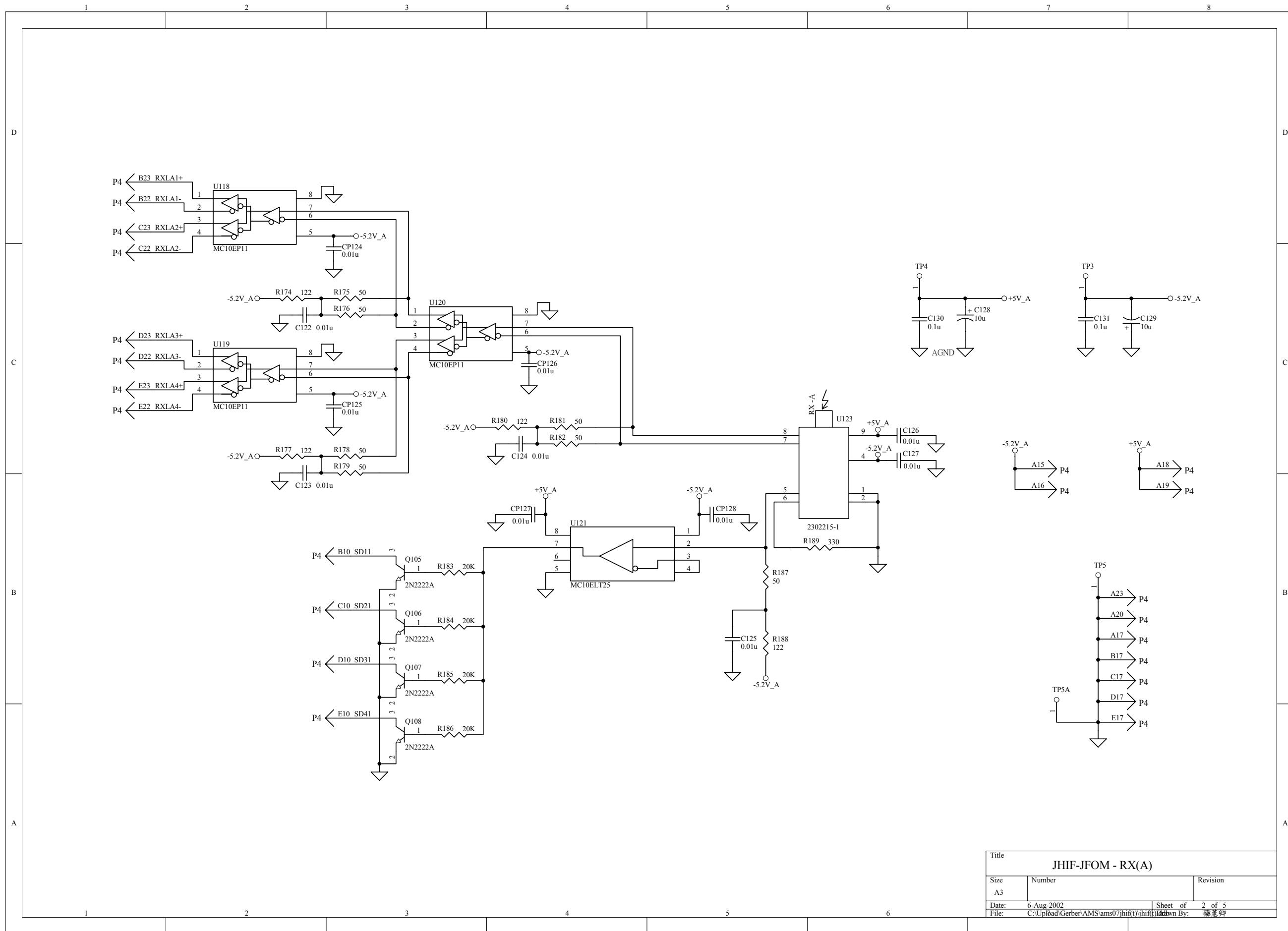
**A.1 Schematic File of the JHIF Board**

**A.2 Layout File of the JHIF Board**

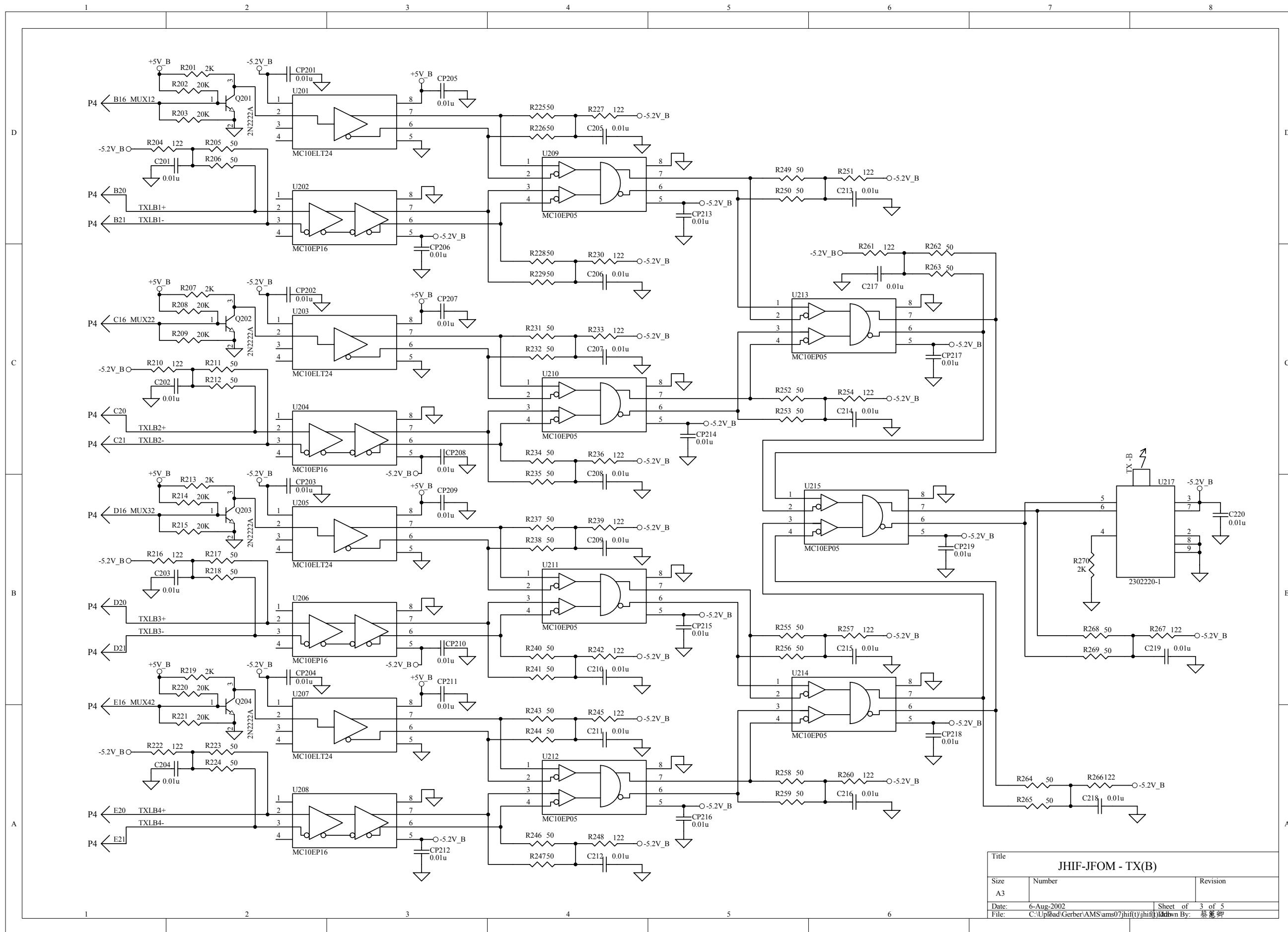
**A.3 BOM File of the JHIF Board**

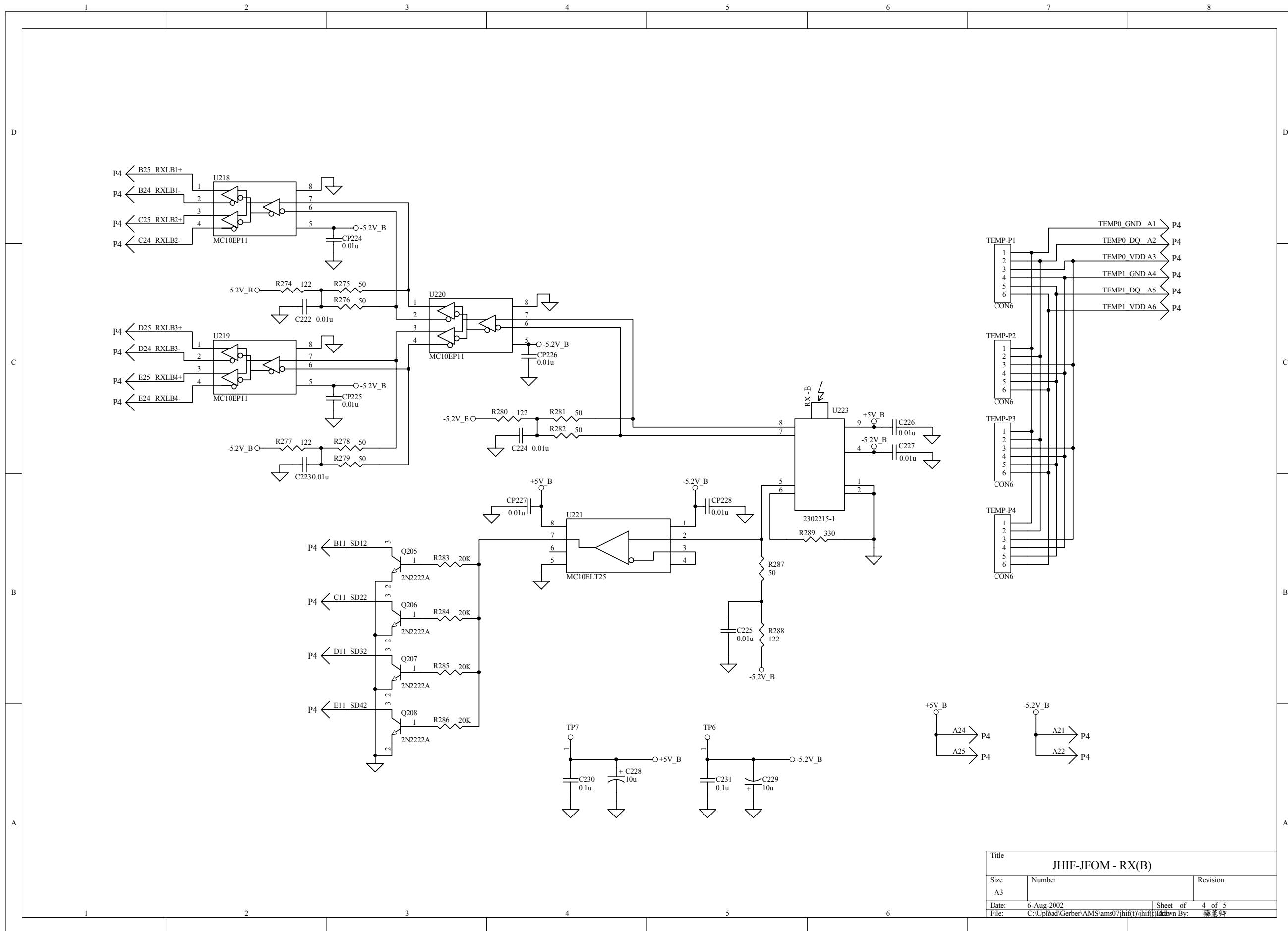
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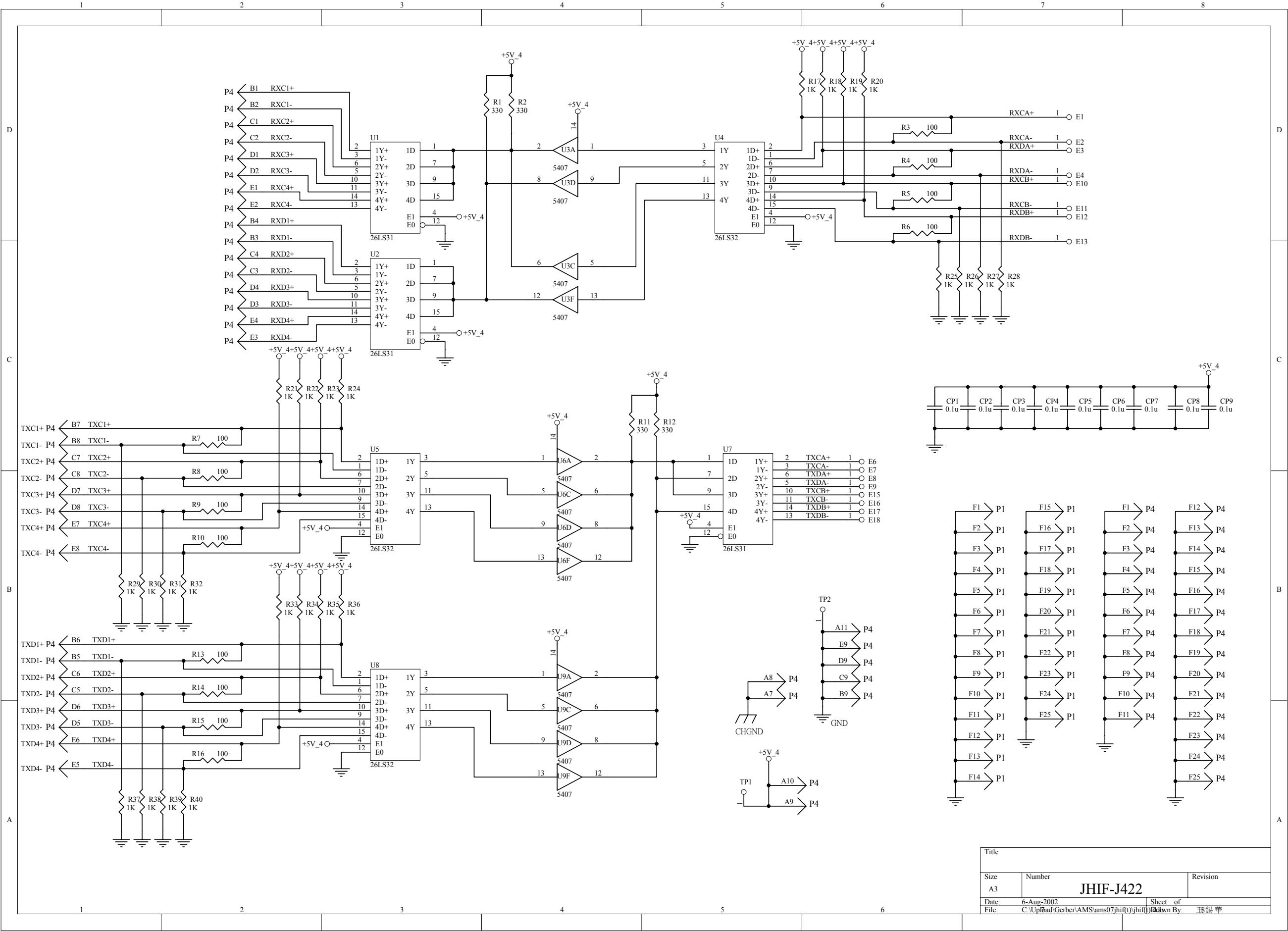


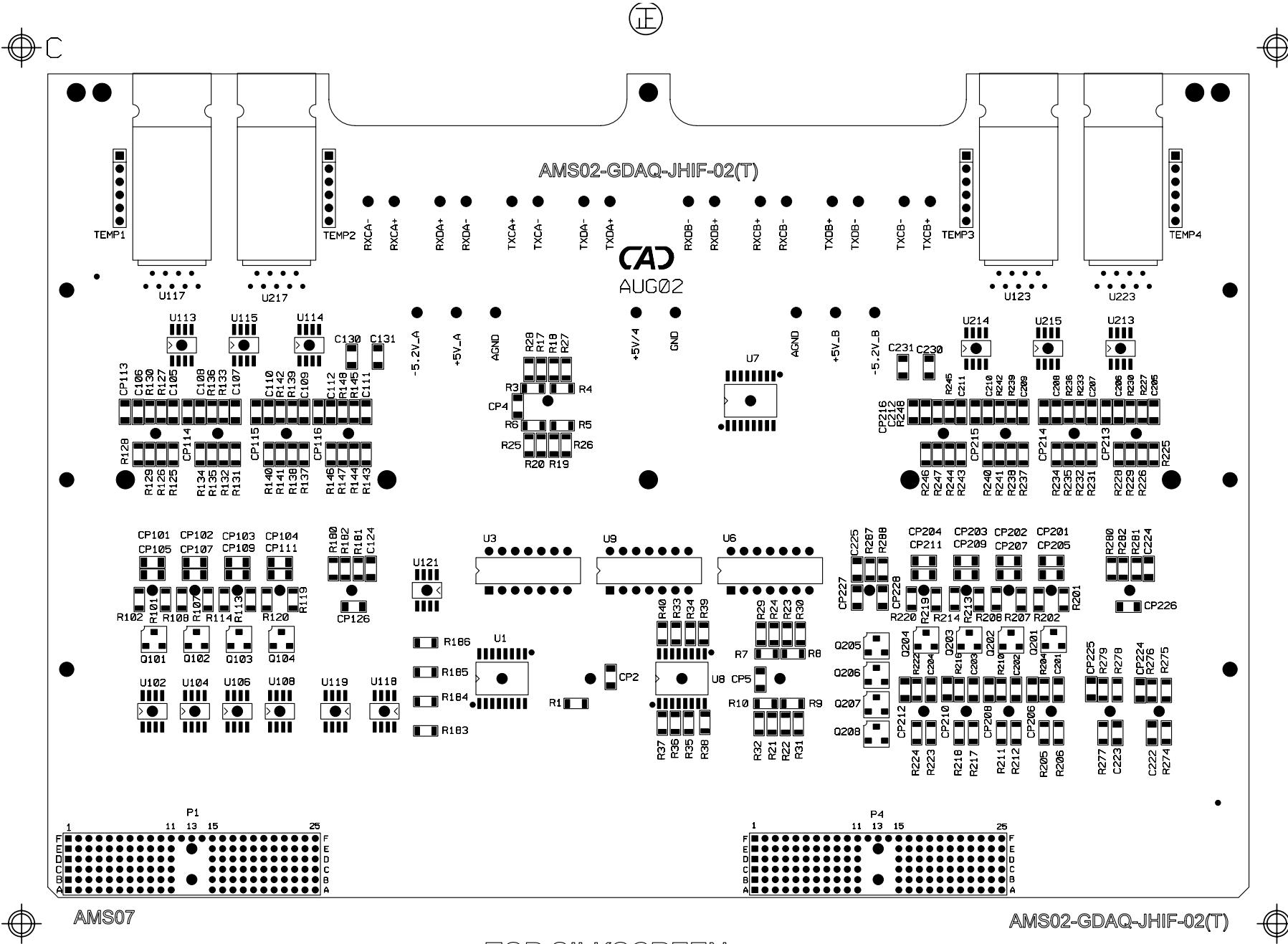
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Size	Number	
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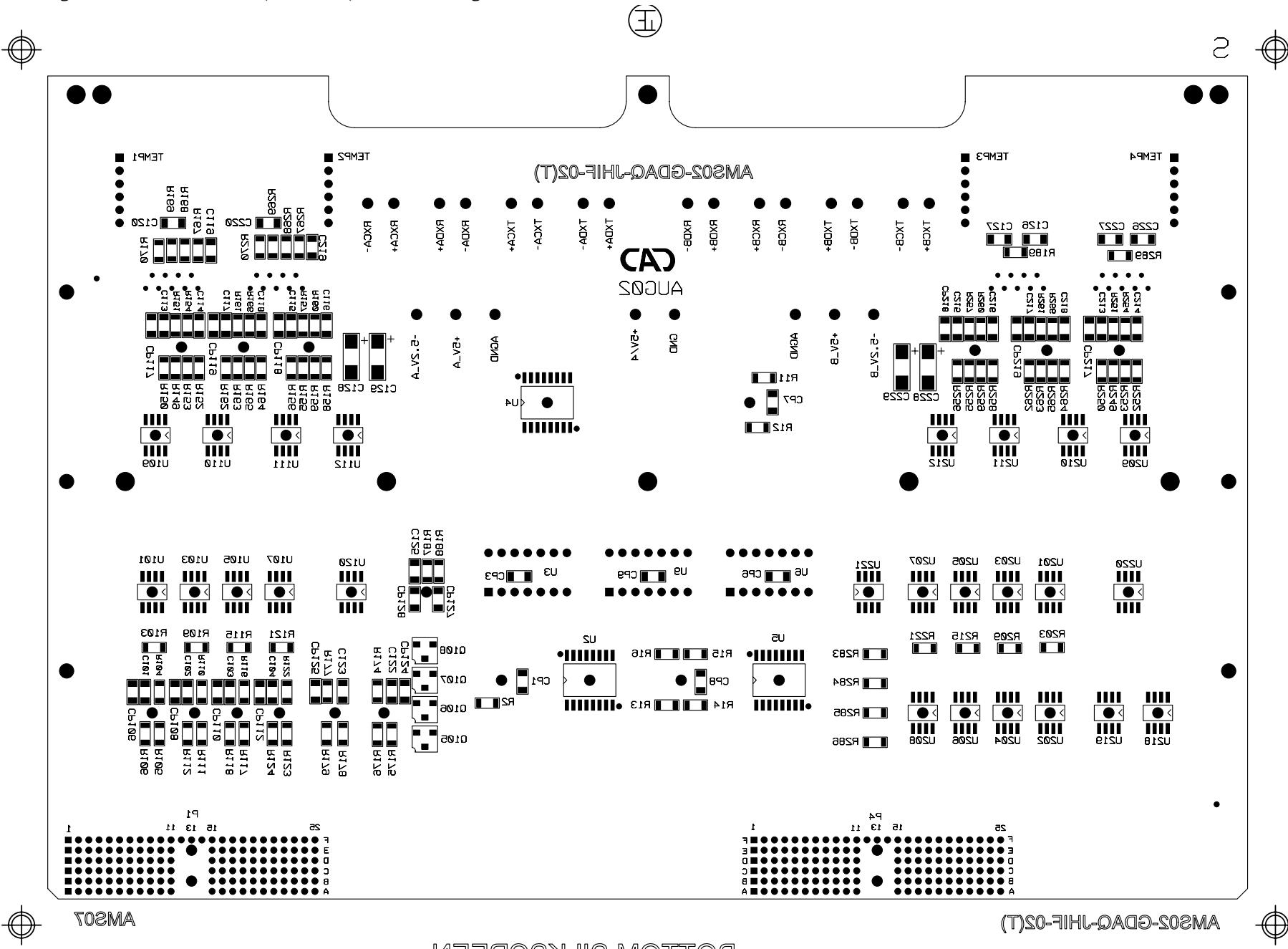


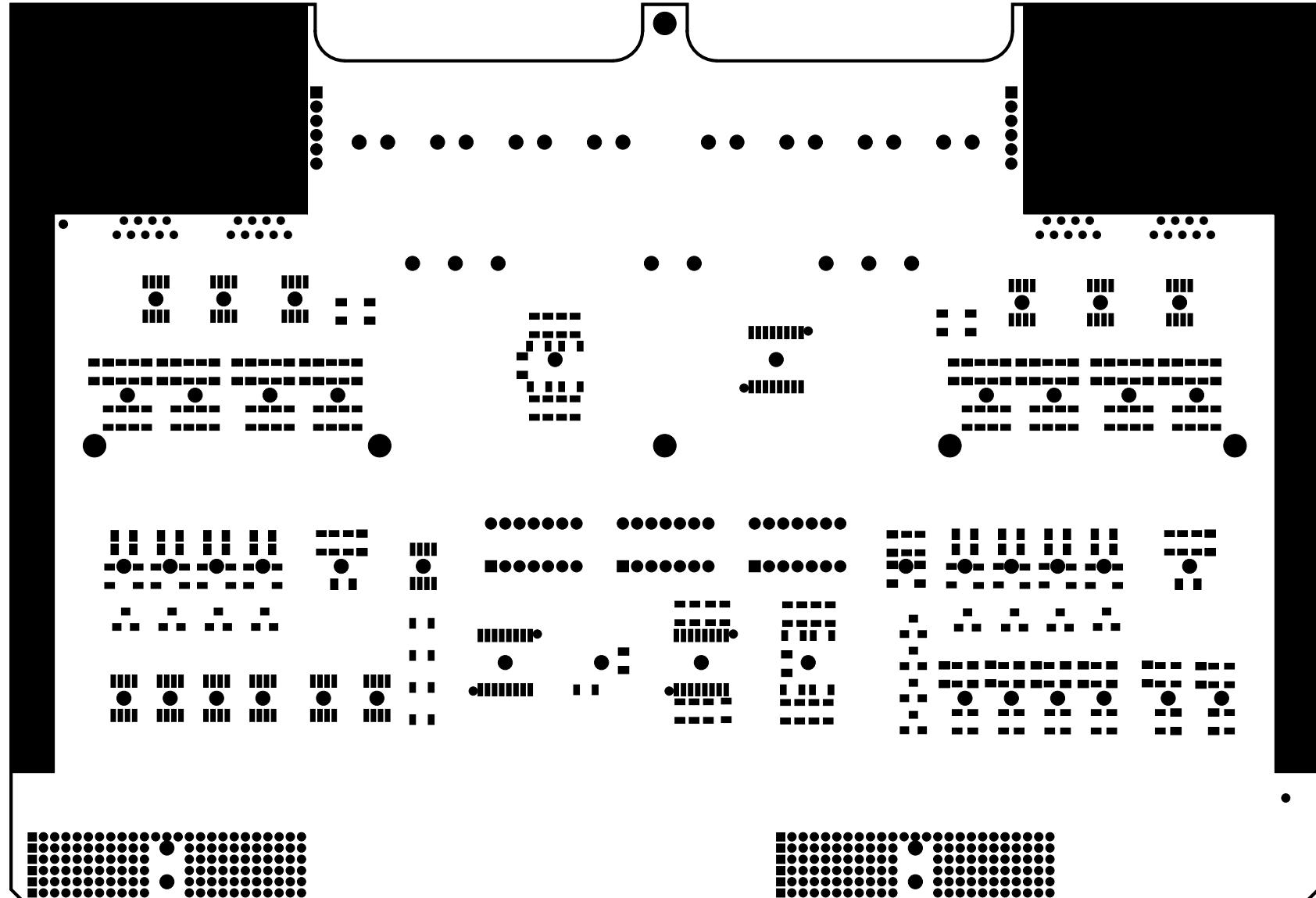
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# TOP SILKSCREEN



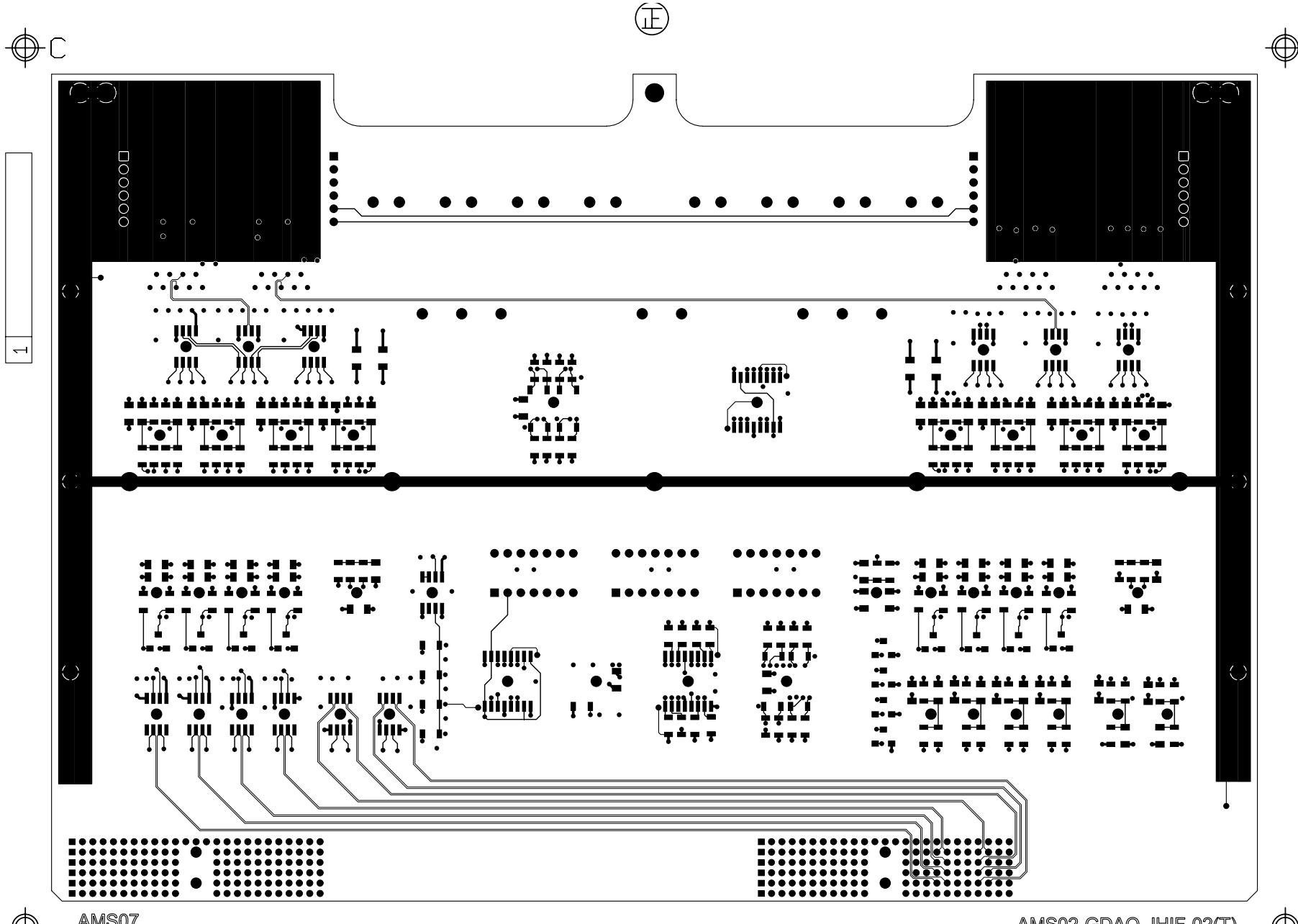


AMS07

## TOP SOLDERMASK

AMS02-GDAQ-JHIF-02(T)

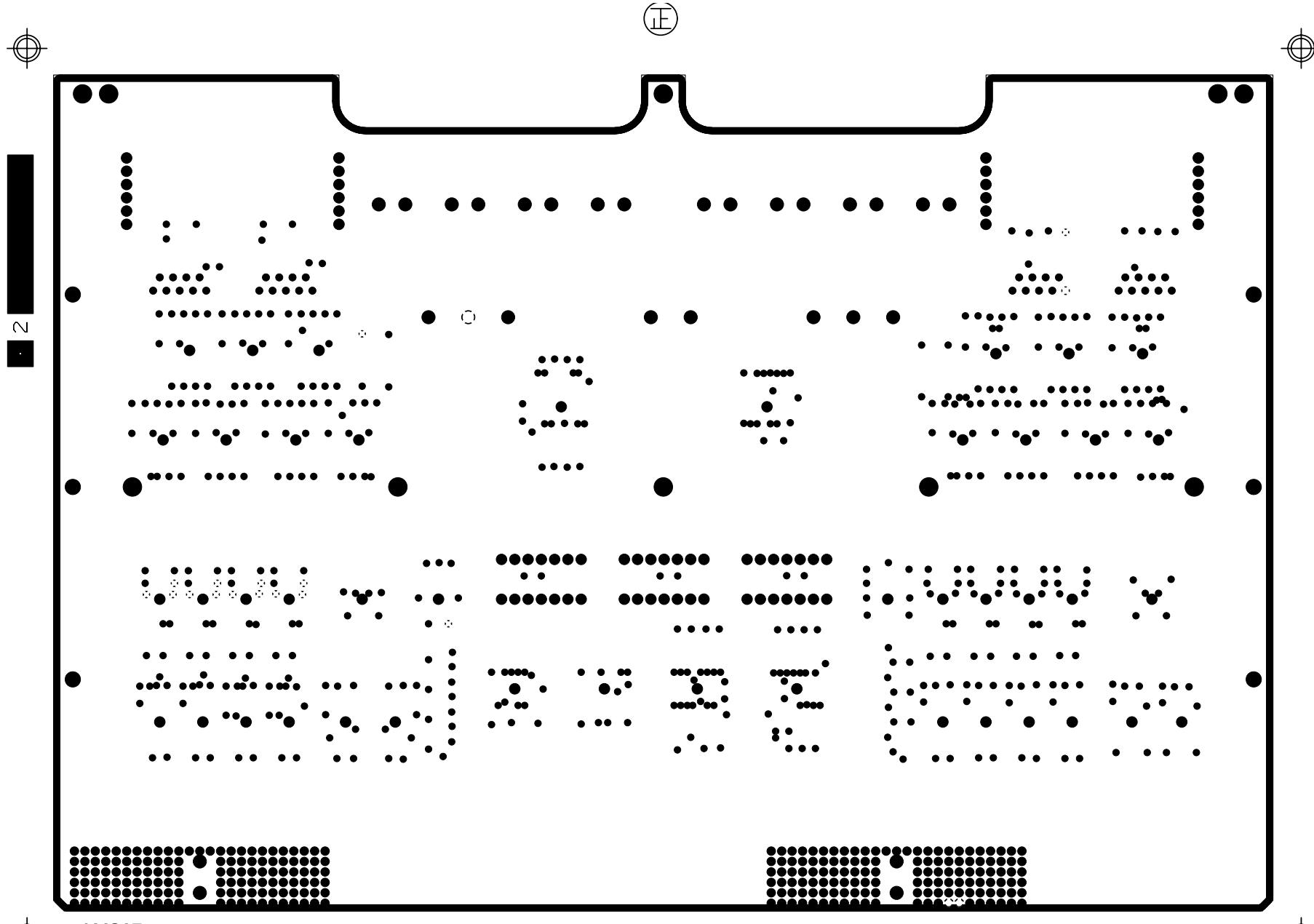




1ST TOP LAYER

AMS07

AMS02-GDAQ-JHIF-02(T)

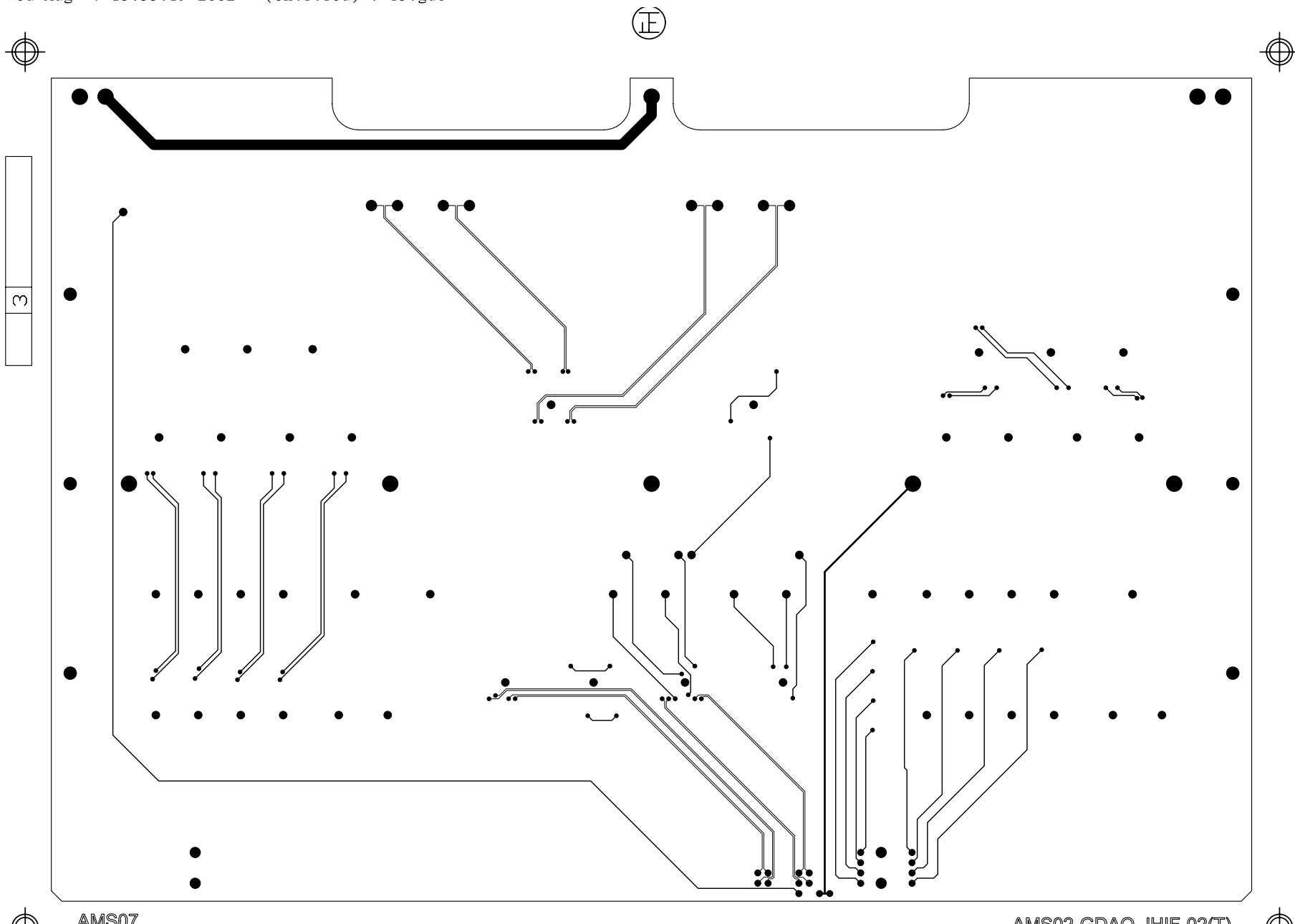


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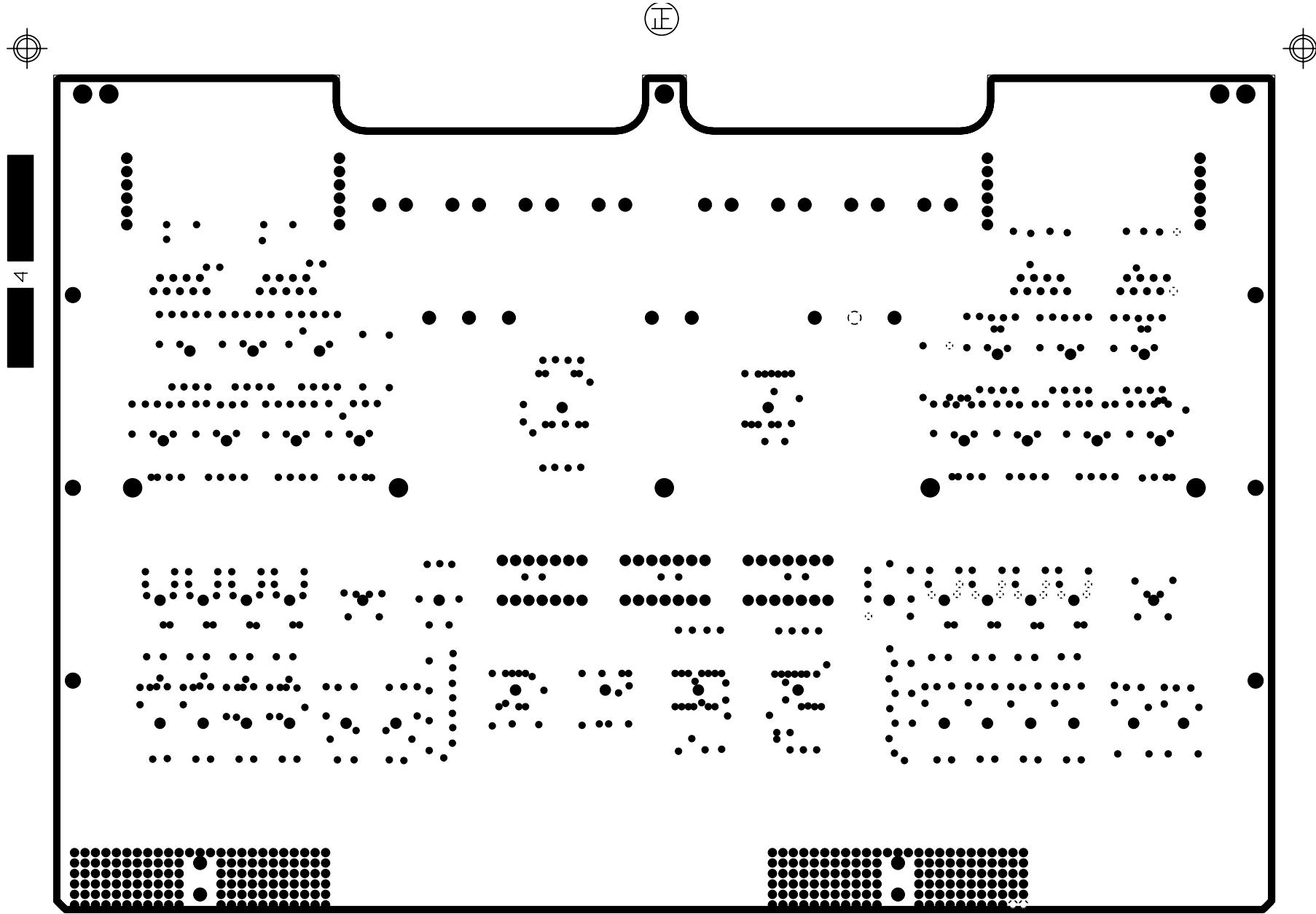


AMS02-GDAQ-JHIF-02(T)

2ND +5V\_A PLANE



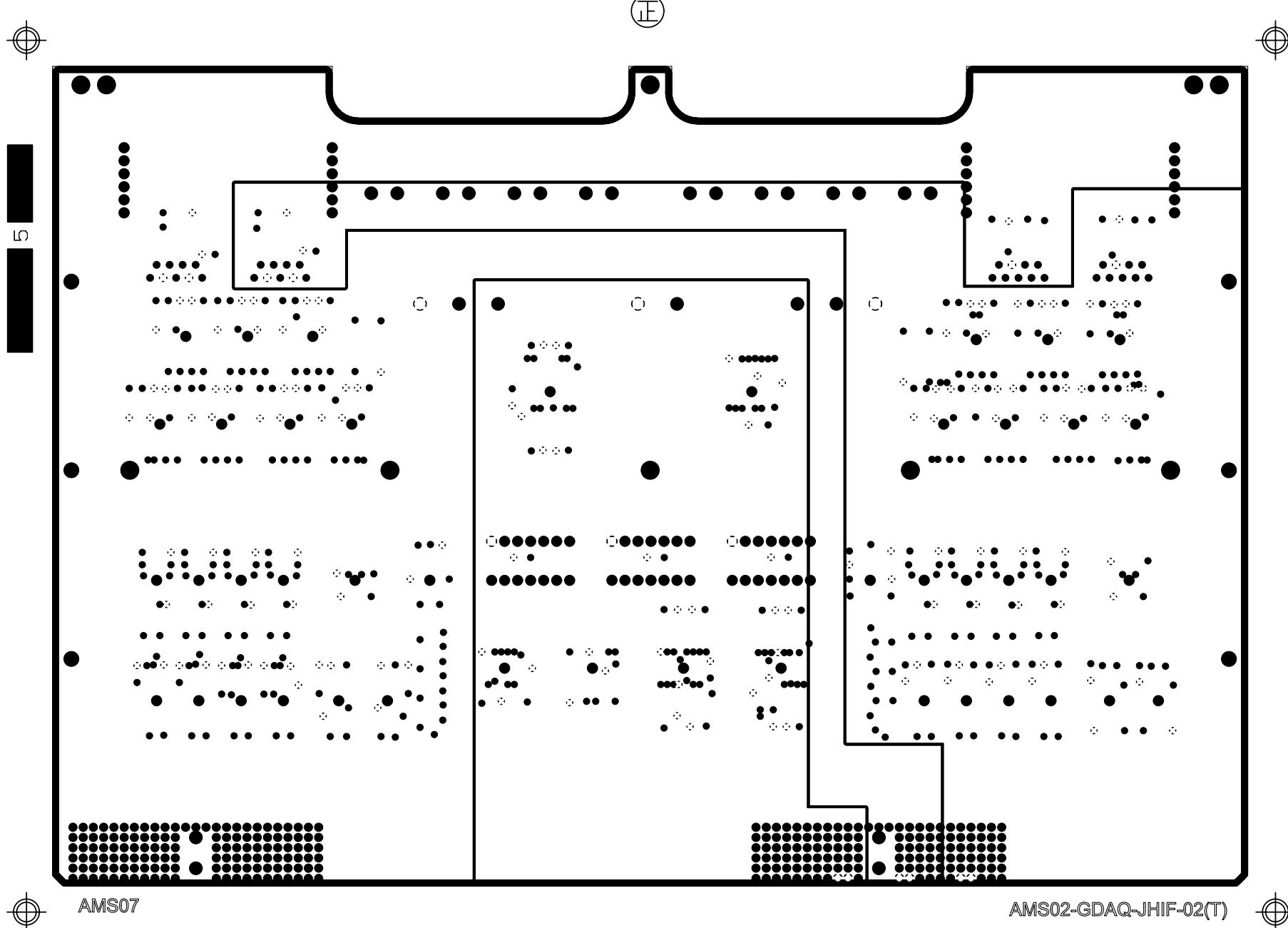
3RD SIGNAL



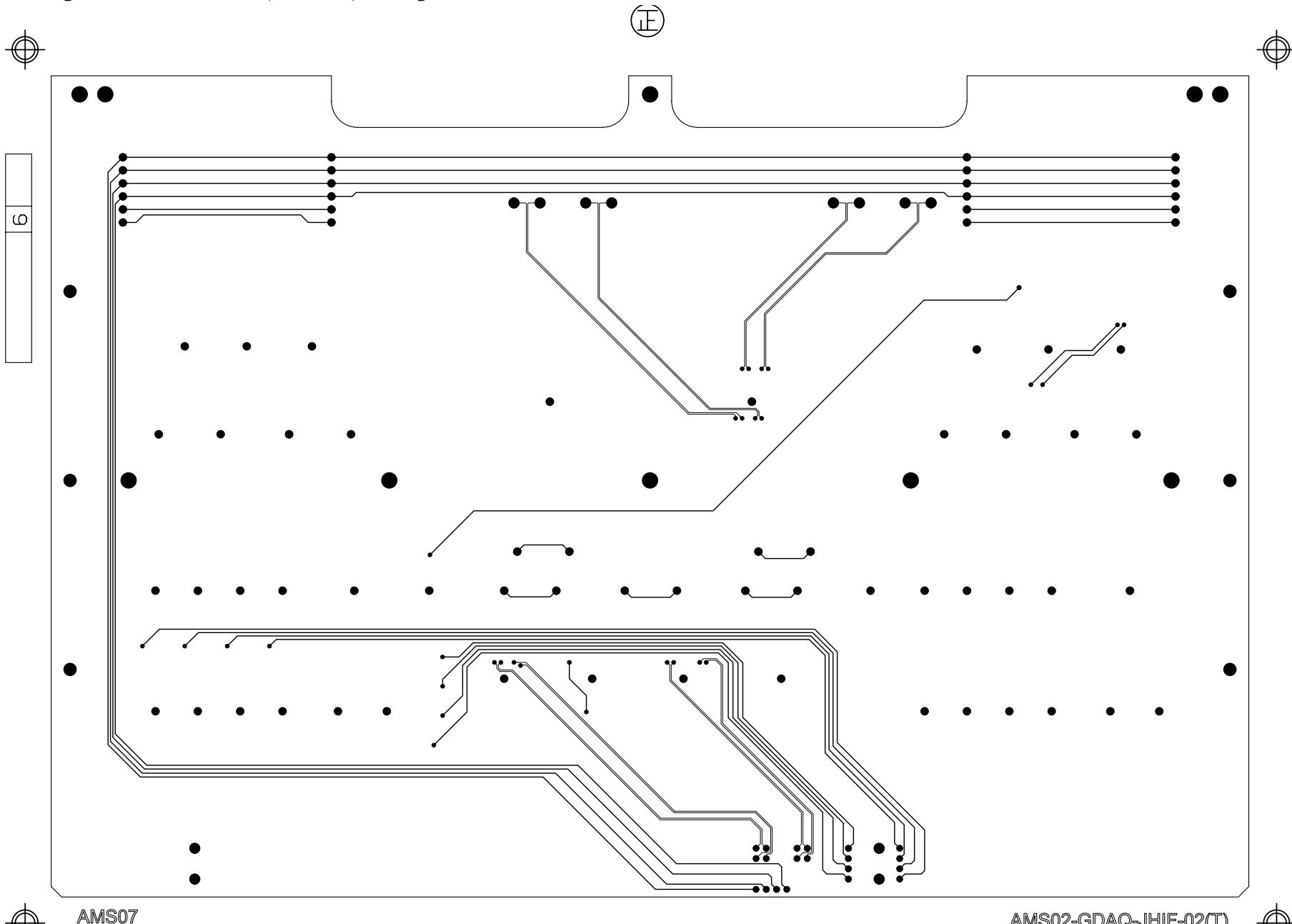
AMS07

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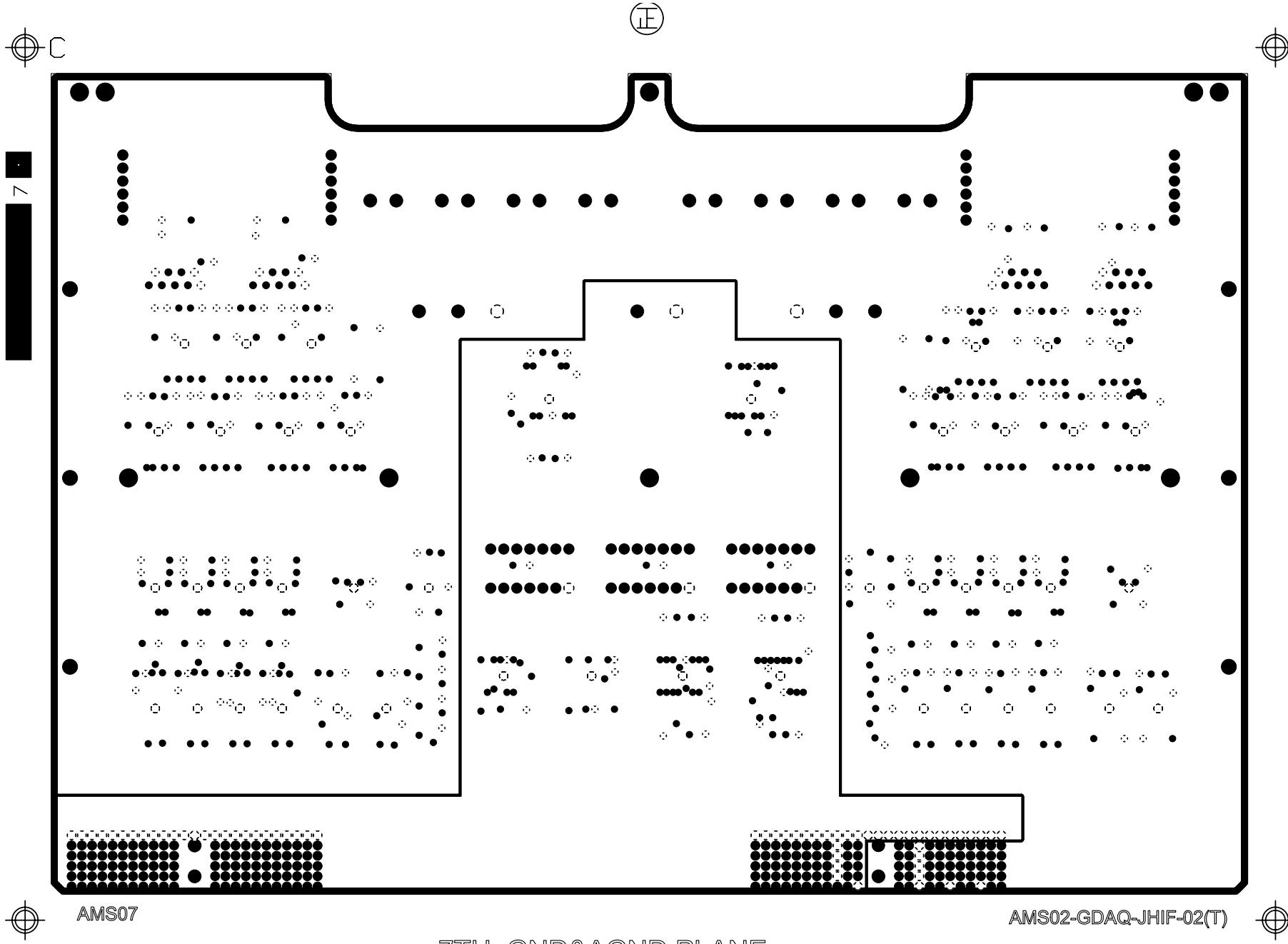
4TH +5V\_B PLANE

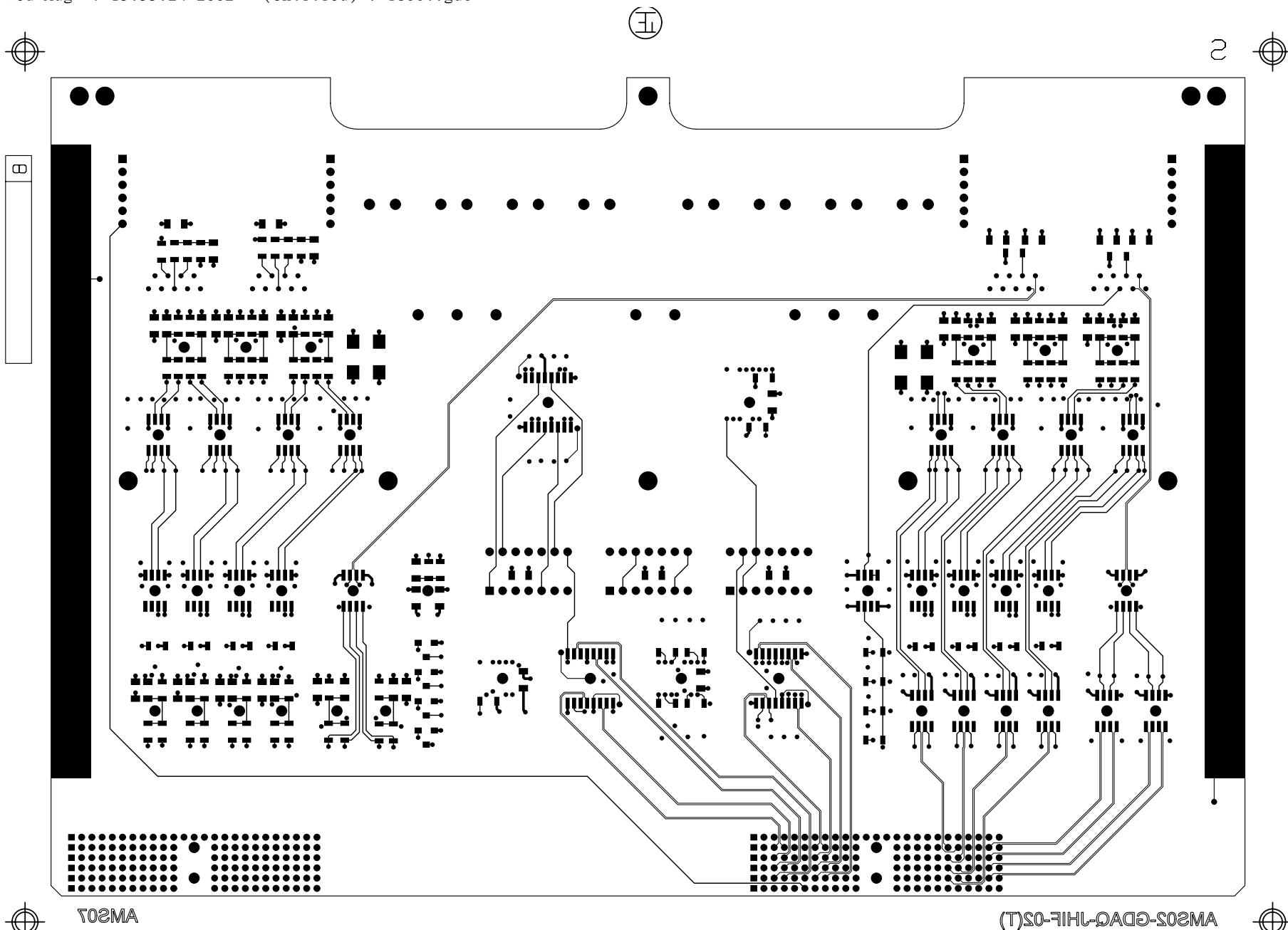


5TH +5V/4&amp;-5.2V\_A&amp;-5.2V\_B PLANE



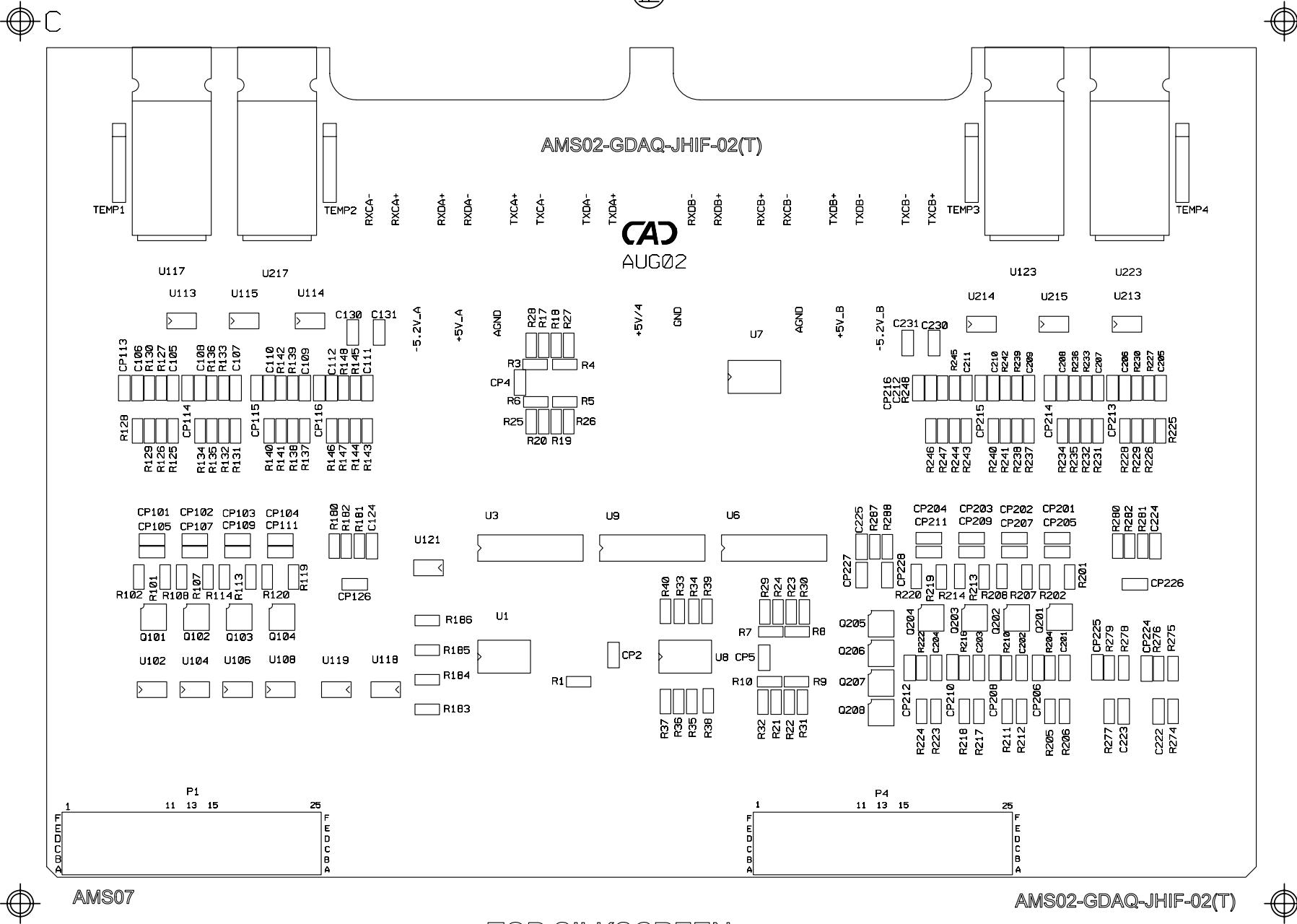
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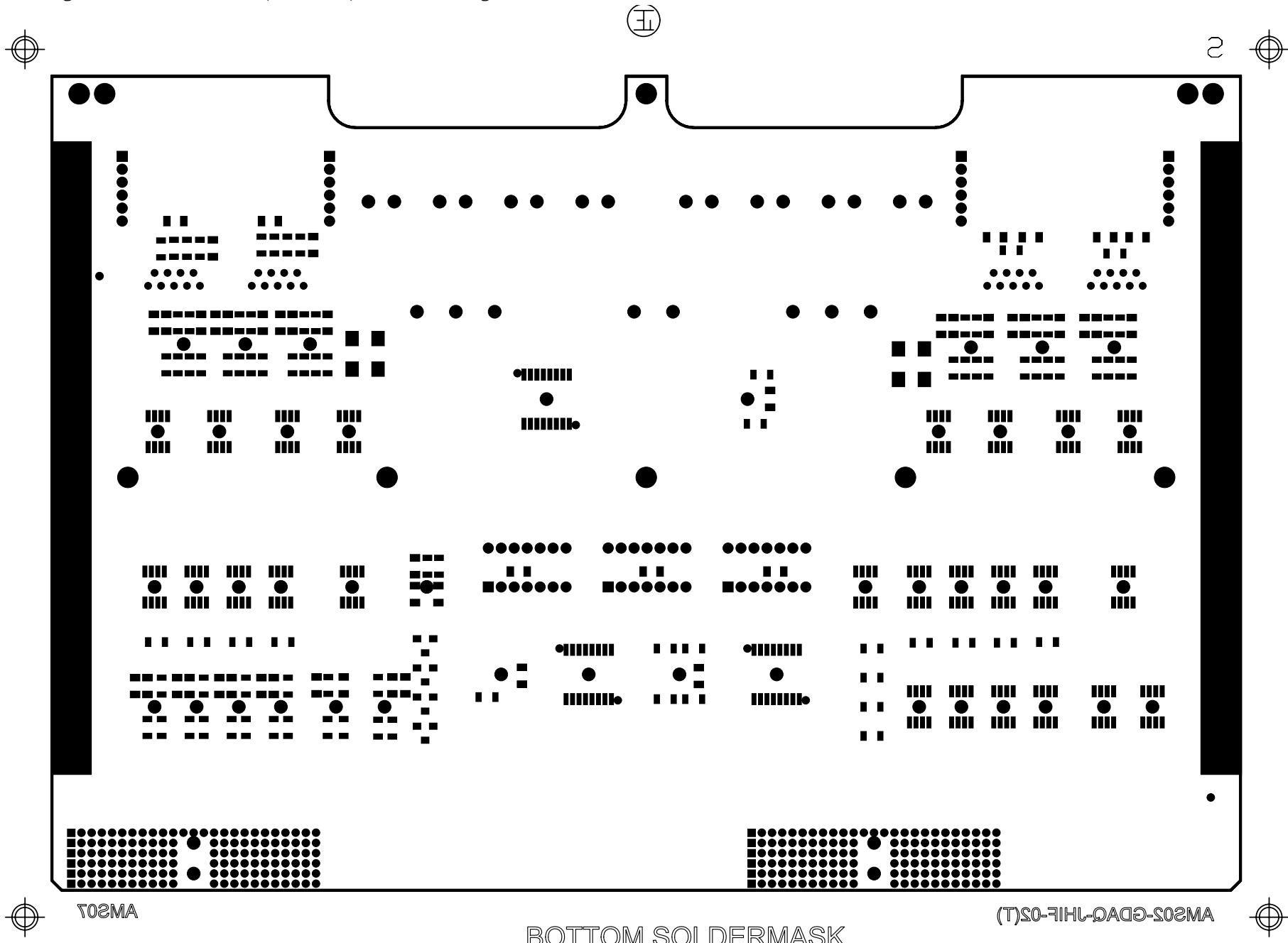


AMS05-GDAG-1HIF-02(T)





## TOP SILKSCREEN



BOTTOM SOLDERMASK

AM202

AM202-GDAG-JHF-02(T)



N N

10

N



AMS07

Symbol	Diameter(in)	Through Holes		Plated	Quant.
		Tolerance(in)	Value		
A	0.010	+0.003	-0.003	Yes	542
a	0.015	+0.003	-0.003	Yes	36
C	0.030	+0.003	-0.003	Yes	270
D	0.036	+0.003	-0.003	Yes	42
E	0.040	+0.003	-0.003	Yes	24
G	0.050	+0.006	-0.006	Yes	24
H	0.060	+0.006	-0.006	Yes	44
K	0.096	+0.006	-0.006	Yes	6
N	0.120	+0.008	-0.006	Yes	10
c	0.080	+0.006	-0.006	No	4

PAD MASTER

AMS02-GDAQ-JHIF-02(T)



Bill of Material for JHIF(T).Bom

Used	Part Type	Designator	Footprint
100	0.01u	C101-C120 C122-C127 C201-C220 C222-C227 CP101-CP119 CP124-CP128 CP201-CP219 CP224-CP228	C1206
13	0.1u	C130 C131 C230 C231 CP1-CP9	C1206
24	1K	R17-R40	R1206
10	2K	R101 R107 R113 R119 R170 R201 R207 R213 R219 R270	R1206
16	2N2222A	Q101-Q108 Q201-Q208	SMA3
4	10u	C128 C129 C228 C229	C6032
24	20K	R102 R103 R108 R109 R114 R115 R120 R121 R183-R186 R202 R203 R208 R209 R214 R215 R220 R221 R283-R286	R1206
3	26LS31	U1 U2 U7	SOIC16W
3	26LS32	U4 U5 U8	SOIC16W
90	50	R105 R106 R111 R112 R117 R118 R123-R126 R128 R129 R131 R132 R134 R135 R137 R138 R140 R141 R143 R144 R146 R147 R149 R150 R152 R153 R155 R156 R158 R159 R162-R165 R168 R169 R175 R176 R178 R179 R181 R182 R187 R205 R206 R211 R212 R217 R218 R223-R226 R228 R229 R231 R232 R234 R235 R237 R238 R240 R241 R243 R244 R246 R247 R249 R250 R252 R253 R255 R256 R258 R259 R262-R265 R268 R269 R275 R276 R278 R279 R281 R282 R287	R1206

12	100	R3-R10 R13-R16	R1206
46	122	R104 R110 R116 R122 R127 R130 R133 R136 R139 R142 R145 R148 R151 R154 R157 R160 R161 R166 R167 R174 R177 R180 R188 R204 R210 R216 R222 R227 R230 R233 R236 R239 R242 R245 R248 R251 R254 R257 R260 R261 R266 R267 R274 R277 R280 R288	R1206
6	330	R1 R2 R11 R12 R189 R289	R1206
3	5407	U3 U6 U9	DIP14
2	2302215-1	U123 U223	FDDI
2	2302220-1	U117 U217	FDDI
4	CON6	TEMP-P1 TEMP-P2 TEMP-P3 TEMP-P4	SIP6
8	MC10ELT24	U101 U103 U105 U107 U201 U203 U205 U207	SOIC8
2	MC10ELT25	U121 U221	SOIC8
14	MC10EP05	U109-U115 U209-U215	SOIC8
6	MC10EP11	U118-U120 U218-U220	SOIC8
8	MC10EP16	U102 U104 U106 U108 U202 U204 U206 U208	SOIC8
1	P1	P1	CON135
1	P4	P4	CON135
24	TP	E1-E4 E6-E13 E15-E18 TP1-TP7 TP5A	TP80